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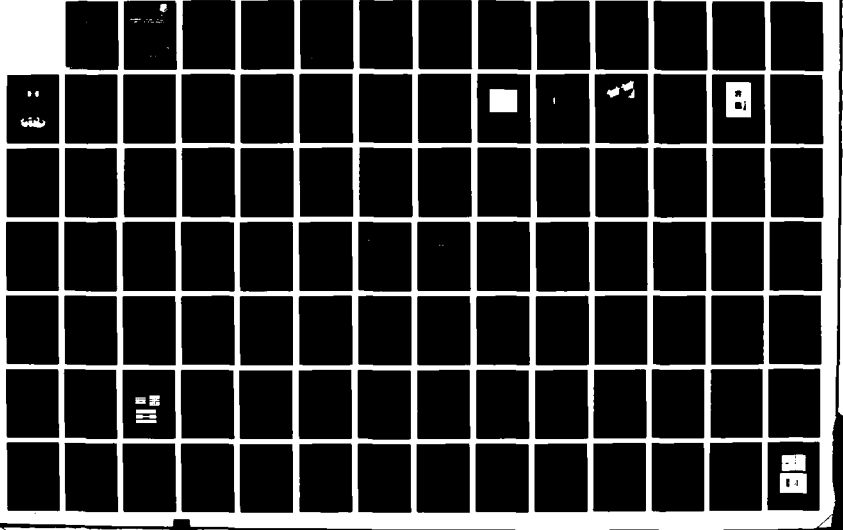

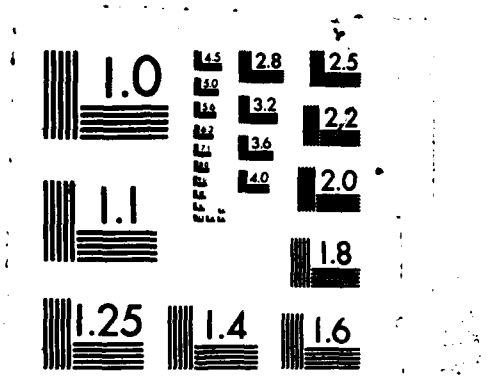

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In-House Report
October 1986

NARROWBAND 10 GHz AND 20 GHz GaAs FET AMPLIFIERS IN COPLANAR WAVEGUIDE

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Single-stage, narrowband 10 GHz and 20 GHz GaAs FET amplifiers using Coplanar Waveguide (CPW) distributed matching elements were built and tested. The amplifiers were constructed to closely model monolithic amplifiers on GaAs by mounting GaAs FET chips into an ϵ_r = 13 substrate material, onto which the CPW matching elements were placed. A CPW test fixture was designed and a routine for de-embedding the s-parameters of FET chips mounted in CPW was developed and successfully used.

The 10-GHz amplifiers had an average of 9 dB gain. Due to a de-embedding error none of the 20-GHz amplifiers provided positive gain at 20 GHz. A second de-embedding effort yielded s-parameters that were used to accurately predict the actual performance of the 20-GHz amplifier designs.

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Preface

The research described in this report is a thesis submitted in partial fullfillment of the requirements for a Masters degree in electrical and computer engineering at the University of Massachusetts. The work was initially performed at the University of Massachusetts and subsequently completed at the Component Technology Branch, Electromagnetics Directorate, RADC.

The author would like to thank Professor Jackson of the University of Massachusetts for his support and help, and Gary Scalzi of RADC for his help with the data acquisition and computer programming aspects of this project.

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1. INTRODUCTION

There is currently a great deal of interest in the construction of millimeter wave phased array antennas using either monolithic or a combination of hybrid and monolithic fabrication techniques. The topics under investigation by various researchers range from the design of the phased array elements and new methods of coupling energy to them, to the possible integration of active devices into the phased array to perform such functions as phase shifting, amplification, or mixing. Much of this research is part of an overall effort to perform technology development relevant to air-to-satellite communications. There would be several advantages to implementing a phased array, active devices, and perhaps a whole transmitting or receiving system in a monolithic fashion on Gallium Arsenide (GaAs). Primarily, large quantities of sophisticated circuits could be produced for a reasonable cost.

The intent of this project was to aid in the above research effort through the design and fabrication of several narrowband GaAs FET amplifiers that use Coplanar Waveguide (CPW) as the transmission line medium. At the two operating frequencies of particular interest for air-to-satellite communications—20 GHz and 44 GHz—feedline losses can substantially limit the gain of a phased array antenna.

(Received for publication 7 October 1986)

These losses can also degrade the noise figure of a receiver using that antenna. An amplifier placed at each element of a monolithic phased array could compensate for these feedline losses. This is the basic motivation for a research effort concerning monolithic amplifiers.

CPW was chosen as the transmission medium because it possesses some potential advantages over microstrip and other transmission lines. Figure 1 depicts a CPW transmission line[1] and the configuration of the electric and magnetic field lines. Both series and parallel elements can easily be attached to CPW, and a CPW line of a given impedance level can be scaled up or down in physical size as required. A CPW feedline, for example, can be made small when appropriate, using up very little "real estate" on a phased array antenna, and then increased in size as necessary in order to be connected to other circuit elements. Conductor losses, however, do vary with the physical dimensions of a CPW line and may impose a limit on the minimum acceptable values of S and W.

It was not feasible at the time this project was initiated, to build truly monolithic amplifiers on GaAs. Instead, a high dielectric constant magnesium-titanate material (TRANS-TECH D-13) was used as a substrate and GaAs FET chips were mounted in it so as to closely model a monolithic environment. Figure 2 is an illustration of the mounting arrangement. A groove the width of the FET chip was cut into the substrate, perpendicular to the CPW line. The FET chip was placed in the groove so that its top surface was flush with that of the substrate. The rest of the groove was filled with Emerson and Cumming K-12 epoxy, and alongside the chip the groove was bridged with gold ribbons to maintain continuity of the CPW ground planes. The FET was electrically connected to the ribbons and the CPW center conductors.

10 GHz amplifiers and 20 GHz amplifiers were built and tested. The 10 GHz amplifiers used the Mitsubishi 1403 FET chip, and the 20 GHz amplifiers used the Mitsubishi 1404 FET chip. All the amplifiers were designed to provide maximum small-signal gain and consisted of a single stage only. Distributed matching elements were used. No attempt was made to actually integrate any amplifiers into a phased array antenna. A test fixture capable of operation beyond 20 GHz was designed, a routine for the RF characterization of FET chips was developed and used successfully, and the 10 GHz and 20 GHz amplifiers were built and tested.

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1. Gupta, K.C. et al (1979) Microstrip Lines and Slotlines, Artech House, Dedham, Massachusetts.

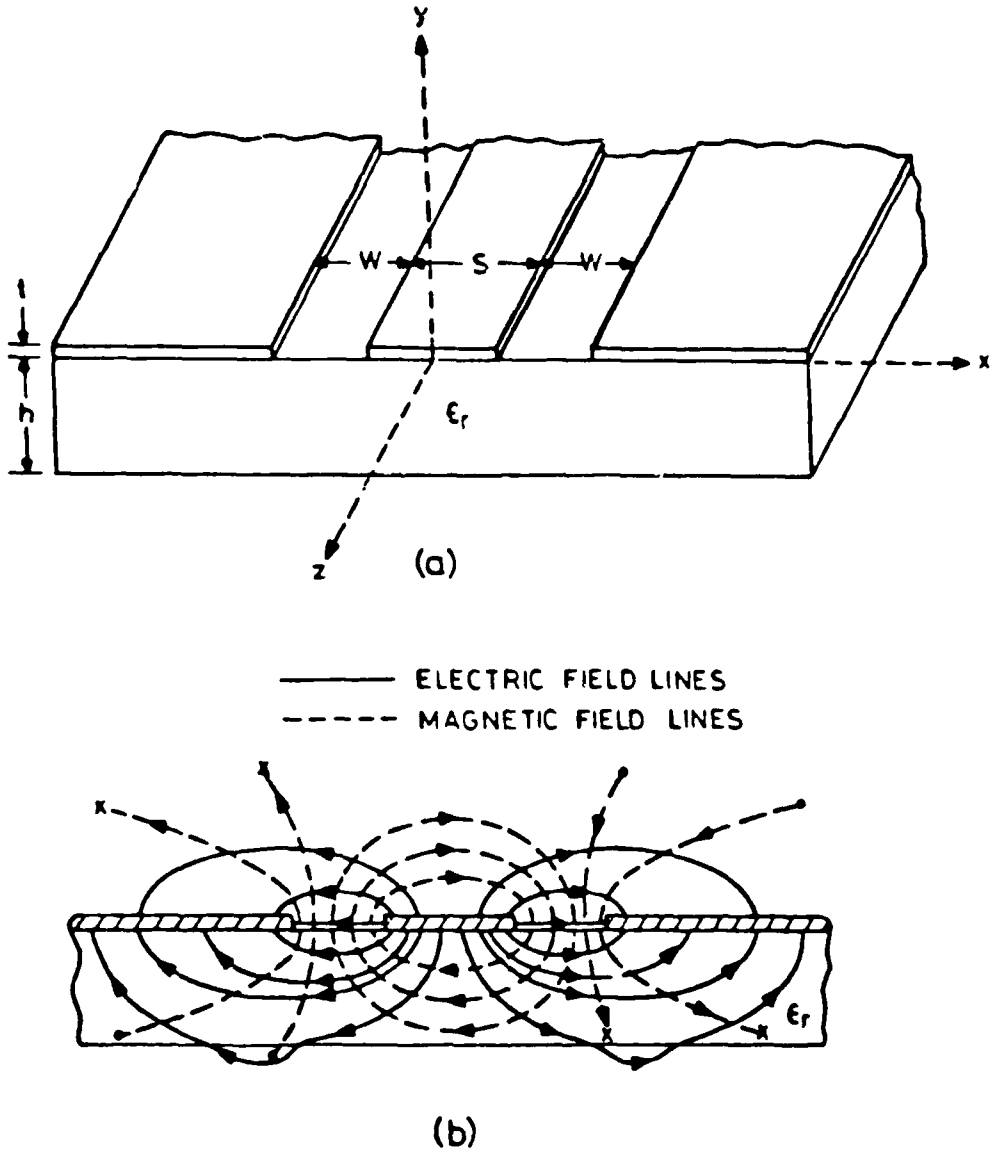

Figure 1. CPW Transmission Line, From Gupta[1]

In Section 2, Coplanar Waveguide is briefly discussed and efforts to build a good test fixture are described. A few different types of transitions from coax to CPW were tried, and sufficiently thin substrates had to be used in the test fixtures to avoid surface-wave generation. The final test fixture used Wiltron female K-connectors and 0.025-in. thick D-13, and behaved well up to at least 26 GHz. The fixtures were approximately 0.800-in. Long, 0.500-in. wide, and 0.750-in. high. Four of these fixtures are pictured in Figure 3. The fixture on the right contains a 10 GHz amplifier.

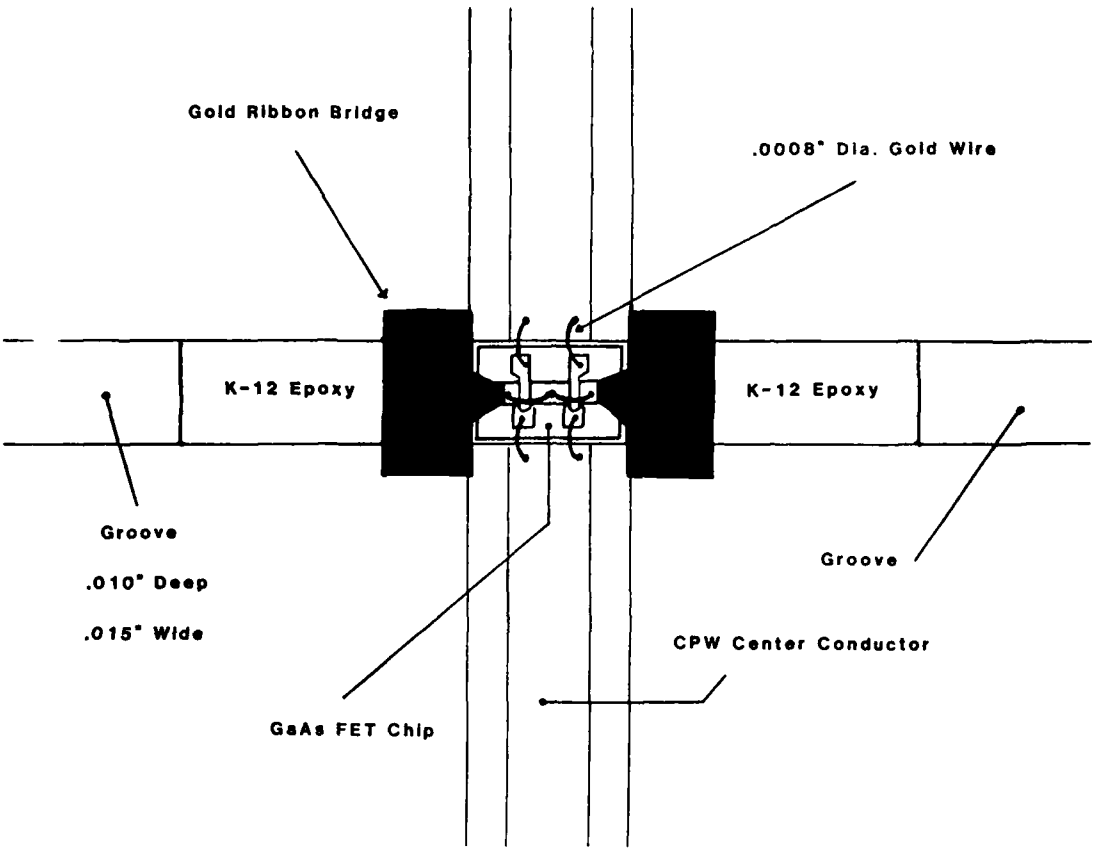

Figure 2. GaAs FET Mounting Arrangement

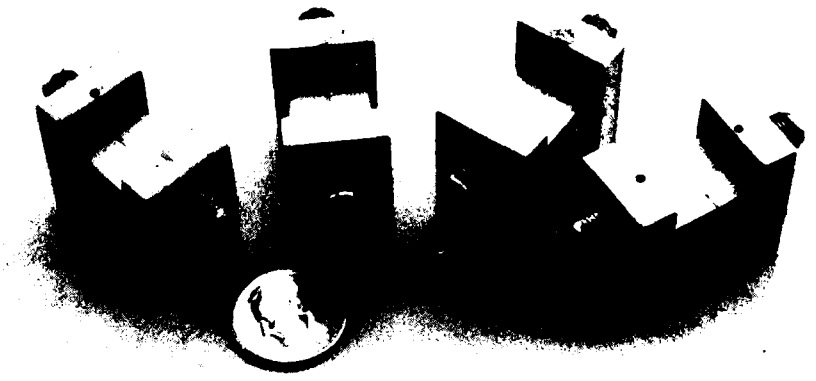

Figure 3. CPW K-connector Test Fixtures

In order to use a semiconductor such as a GaAs FET to its fullest potential, it is necessary to have an accurate knowledge of its electrical characteristics. In this project, the active device is viewed as a two-port box capable of signal gain. The interior of the box is not considered in any detail. The primary electrical characteristics required are the s-parameters of the two-port for the frequency range over which it is capable of gain. GaAs FET s-parameters can depend heavily on the manner in which the chip is mounted into its circuit. Because the s-parameter values published by the manufacturer are for FET chips mounted in microstrip, not in CPW, it was necessary to measure the s-parameters of the 1403 and 1404 FET chips in the lab. This is not necessarily trivial. The network analyzer measures not only the FET chip, but the surrounding test fixture and connectors as well. It is necessary to "de-embed, or extract from the measured data, the actual s-parameters of the FET chip. At low frequencies (for example, 2 GHz) this is often done by assuming the test fixture and its connectors behave as ideal transmission lines, but at the frequencies of interest in this project, that assumption is not valid. Section 3 explains the de-embedding procedure used in this report, and Section 4 presents the s-parameters obtained.

Most of the equations used in the design of the 10 GHz and 20 GHz amplifiers are based on the chip's s-parameters and can be found in various textbooks, and are programmed on the computer-aided design program SUPERCOMPACT.® [2, 3, 4] The design and performance of the 10 GHz and 20 GHz amplifiers are reviewed in Section 5, and the use of the relevant equations is discussed. The graphics capabilities of SUPERCOMPACT® were found to be very useful, and the program was used for optimization as well. Although SUPERCOMPACT® can account for discontinuities and edge effects in microstrip, it does not yet possess this capability for CPW. Discontinuities presented some problems and were taken into account as best as possible in the design of the amplifiers. This is discussed in Section 5. Conclusions and recommendations are presented in Section 6.

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2. Gonzalez, G. (1984) Microwave Transistor Amplifiers, Prentice-Hall, Inc., Englewood Cliffs, New Jersey.

3. Ha, T. T. (1981) Solid State Microwave Amplifier Design, John Wiley and Sons, New York.

4. Vendelin, G. D. (1982) Design of Amplifiers and Oscillators by the S-parameter Method, John Wiley and Sons, New York.

2. COPLANAR WAVEGUIDE AND TEST FIXTURE DEVELOPMENT

2.1 Coplanar Waveguide

A Coplanar Waveguide (CPW) transmission line, shown in Figure 1, has some unique characteristics that make it potentially advantageous to other types of transmission lines for certain applications. The characteristic impedance of a CPW line depends mainly on the ratio of the center conductor width, S in Figure 1, to the width of the center conductor and the slots combined, S+ 2W. As a result, the size of a constant impedance CPW line may be adjusted to optimize a particular circuit design. CPW lines may be made small (within limits) when conserving "real estate" is important, or can be made whatever size is best to connect to other circuit elements. Through the use of a taper of a constant impedance, the same line can be scaled up and down as many times as required. Another advantage of CPW is the ease with which it can accommodate both parallel and series circuit elements, because the ground planes and the center conductor are on the same side of the substrate. Microstrip, for example, often requires a plated-through hole or wrap-around metallization to make a connection to ground. CPW can also display less dispersion than microstrip.

The electric and magnetic field lines of CPW are shown in Figure 1b. When both the ground planes are at the same potential with respect to the center conductor, as is the case in Figure 1b, the CPW is said to be excited in the odd mode. The CPW lines used in this project were intended to be used in this mode.

The properties of a transmission line that are of the most importance for the narrowband amplifier designs of this project are the characteristic impedance, ZO, the effective dielectric constant, Keff, and the attenuation constant for travelling waves, α. There are several different methods by which ZO, Keff, and α can be calculated for CPW and other transmission lines. Gupta[1] gives a good description of the methods that have been applied to CPW and discusses the results of each. He describes a quasi-static approach, a modified quasi-static approach, and full-wave techniques such as Galerkin's method in the spectral domain. The simplest quasi-static solution assumes an infinitely thick substrate and a metallization of zero thickness. With modifications, the quasi-static technique can account for finite substrate and metallization thicknesses, and can predict conductor and dielectric loss. The solutions can be written in closed form. The quasi-static approaches, however, are all "zero-frequency" methods, that cannot predict dispersion or account for power radiated into any of the surrounding dielectric media. The full-wave analyses are much more rigorous than any of the quasi-static methods. While they can predict dispersion and do include the effects of power radiated away, they often require extensive numerical calculations on a computer. The TRL option of

the program SUPERCOMPACT® also contains a routine for calculating the ZO, Keff, and α of CPW lines. This routine allows for the input of the center conductor width (S), slot width (W), substrate thickness (H), relative dielectric constant (EFF), the loss tangent of the dielectric (TAND), the surface roughness of the substrate (RGH) and up to three metallization layers, each of a different thickness. Grounded CPW (GCPW) and CPW in a waveguide can also be analyzed.

Plots of the ZO and Keff of CPW lines as a function of S, W, EFF, and H were generated from SUPERCOMPACT® and found to agree with the plots presented in Gupta based on the modified quasi-static technique of Davis.[1] This agreement is shown in Figure 4. The calculations of SUPERCOMPACT® were also compared

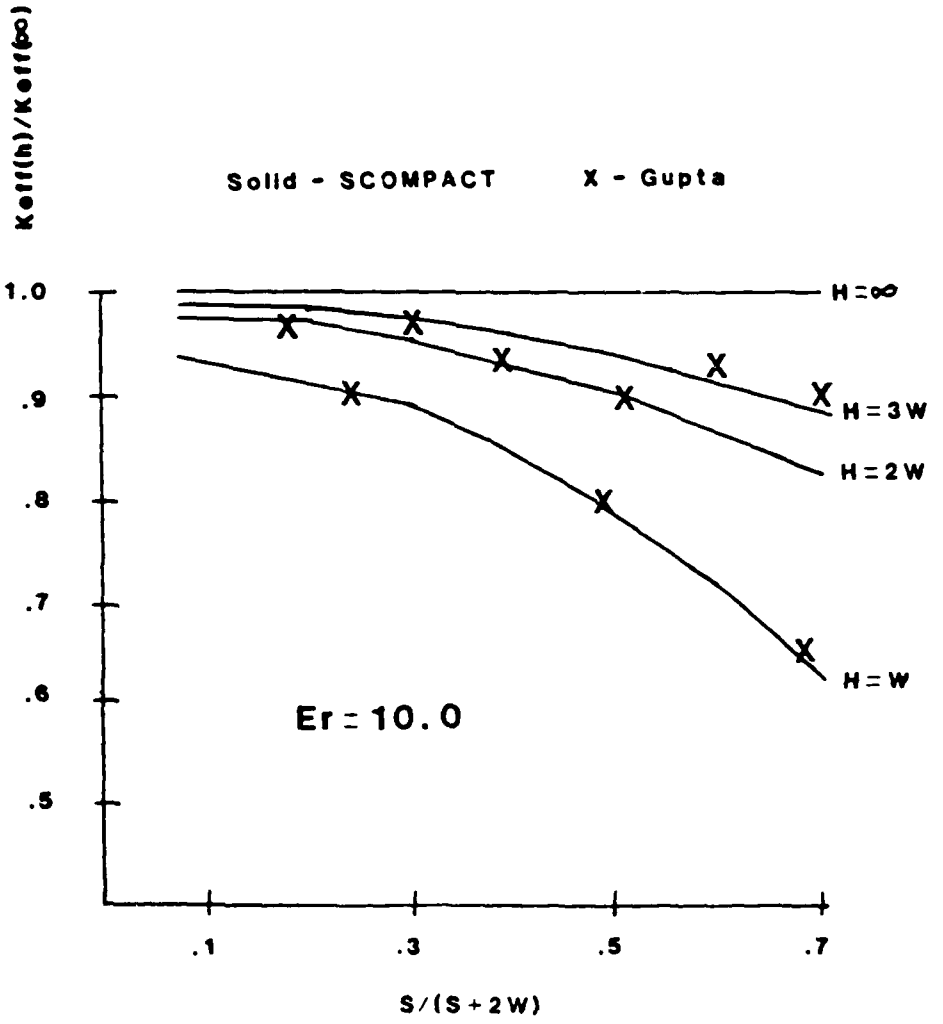

Figure 4. SUPERCOMPACT® and Quasi-static Predictions of CPW Effective Dielectric Constant

with a full-wave solution presented in Gupta. The results of this comparison are shown in Figures 5 and 6. The full-wave solution is that of Knorr and Kuchler.[1] Any result from SUPERCOMPACT® is independent of frequency and will not vary with H/λ_o. In Figures 5 and 6, W/H is equal to 0.25, which is very close to the value used for all the 50-Ω lines in the amplifier designs. There is no significant difference in the impedance predictions between SUPERCOMPACT® and the full-wave solutions for values of S/H less than one. An increase in frequency has a noticeable effect on the difference between the guide wavelength calculations in Figure 6.

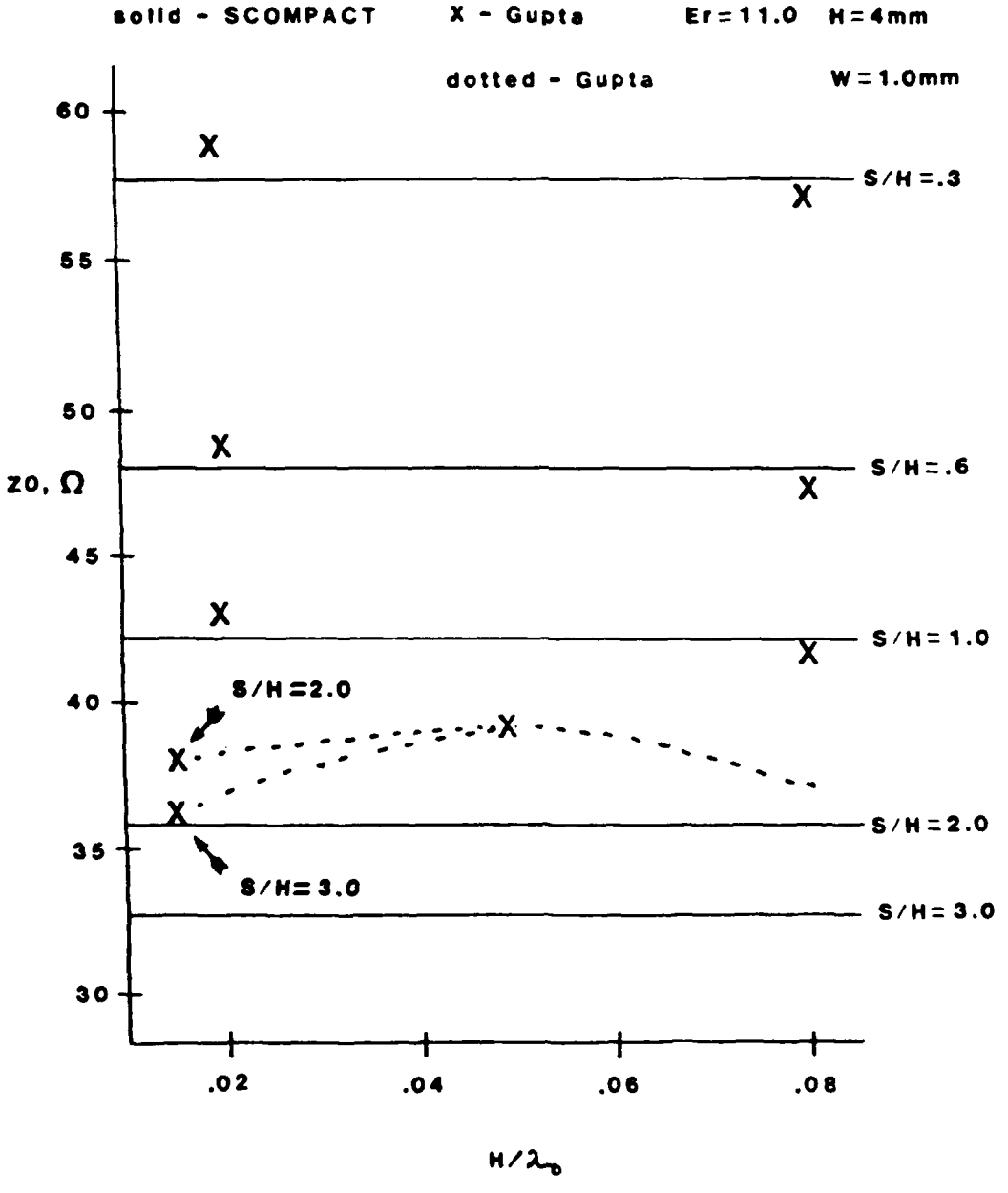

Figure 5. SUPERCOMPACT® and Full-wave Predictions of CPW Impedance

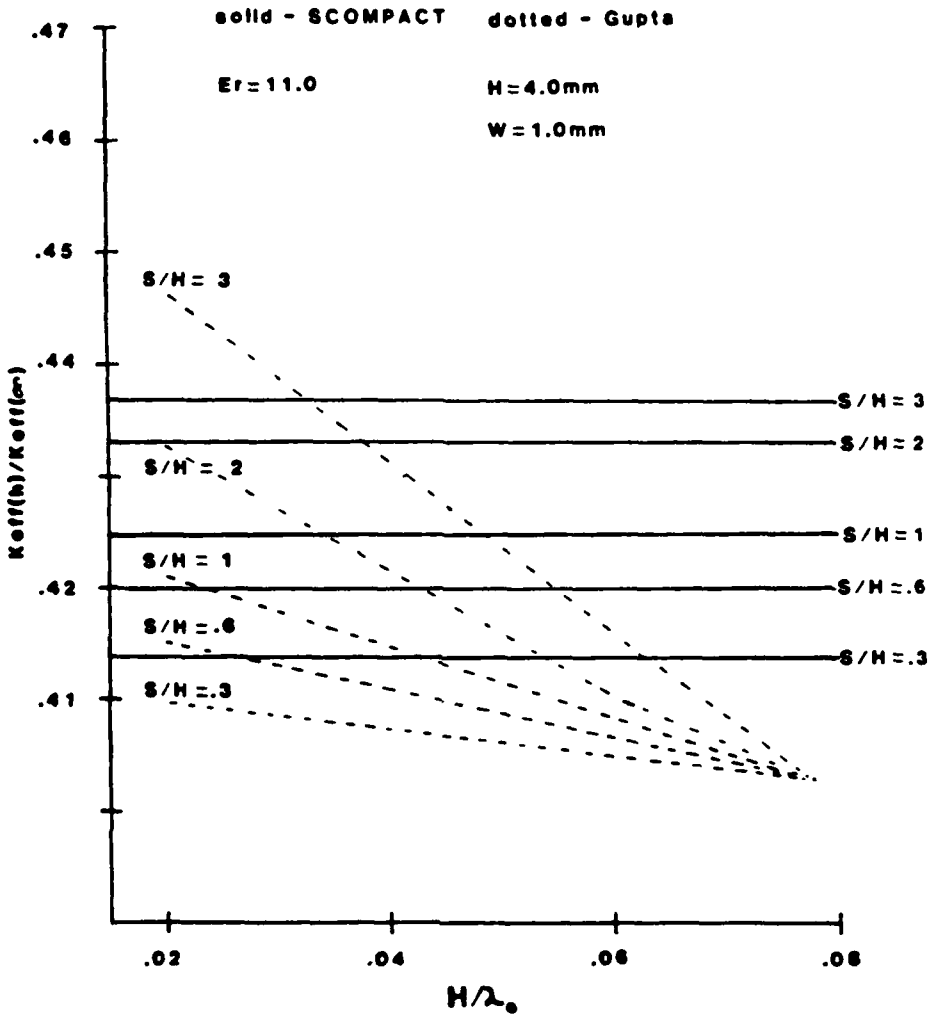

Figure 6. SUPERCOMPACT® and Full-wave Predictions of CPW Effective Dielectric Constant

Most of the CPW lines used in this report were designed using SUPERCOMPACT,® mainly because of the ease of obtaining a fast solution, but also because the differences between SUPERCOMPACT® and the full-wave solution were not great for the values of line parameters used. The design of the 10 GHz amplifiers relied solely on SUPERCOMPACT® to determine the CPW characteristic impedances and the electrical lengths. These amplifiers performed adequately. In the 20 GHz designs, SUPERCOMPACT® was used for the impedance calculations, but the electrical lengths of the CPW lines were determined using a value of Keff 5 percent higher than that supplied from SUPERCOMPACT®. This percentage was arrived at from a comparison of SUPERCOMPACT®'s calculation of Keff of a 50-Ω line with the Keff of the same line calculated at 20 GHz using a full-wave solution.

2.2 Test Fixture Development

Most modern equipment used for network analysis at microwave frequencies requires a device under test to be terminated in SMA or APC-7 type test connectors. Therefore, it was necessary to find a good electrical transition from coax, which is trivial to convert to SMA or APC-7, to CPW. Also, a test fixture had to be developed that allowed GaAs FET chips mounted in CPW, as well as the final amplifiers realized using CPW, to be accurately characterized. Any test fixture would necessarily consist of back-to-back transitions, and contain a sufficient length of CPW line to allow space for a FET chip and for the amplifier matching elements. The term "back-to-back" refers to a coax-to-CPW transition followed by a CPW-to-coax transition. There are several performance criteria that a good test fixture must meet. First, the transitions should reflect as little as possible of the energy incident upon them, and the fixture should have as low as possible insertion loss. All of the energy incident upon the test fixture should be coupled into the transmission line mode on the CPW; very little energy should be lost to surface wave propagation in the substrate material or coupled into any possible resonant modes that may exist due the particular configuration of the test fixture. A return loss plot over frequency of a test fixture containing a 50-Ω line should consist of periodic maxima and minima resulting from the constructive and destructive superposition of small reflections from the transitions at each end of the fixture. The insertion loss should result from attenuation of the travelling waves along the CPW and may show a ripple corresponding to mismatch loss. Any substantial deviation from the ideal curves indicates potential problems could exist in extracting good data at that frequency from a FET chip or an amplifier mounted in a similar test fixture.

The de-embedding routine used to characterize the FET chips required a fairly low reflection from the test fixture transitions in order for assumptions that simplified the mathematics to be valid. It was felt that a maximum return loss of 15 dB or more for frequencies up to and including 12 GHz from a test fixture consisting of two transitions separated by a length of 50-Ω line would indicate an acceptable transition from coax to CPW. The goal at 20 GHz was rather arbitrarily set at 10 dB; basically, the best that could be accomplished with a reasonable effort would have to be accepted. The return loss of a single transition can be approximated as 6 dB less than the maximum from two back-to-back transitions. This is valid for two electrically identical, lossless transitions connected by a length of lossless transmission line.

2.2.1 TRANSITIONS TO CPW

Initial tests of CPW lines used 0.063 in. and 0.133-in. thick D-13 substrates that were obtained from TRANS-TECH. Chrome was deposited onto the substrates as the first metallization layer using a CVC 164 evaporator system. Gold or copper was used as a top layer. Electroplating was used to increase the thickness of the top layers to at least 100 micro-inches. Various CPW lines were then etched. A transition similar to a type found in the literature was tried first.[5] An SMA connector was attached to one end of a piece of semi-rigid coaxial cable, and the cable was soldered or epoxied to the CPW lines etched on the D-13. Figure 7 is an example of one of the test substrates and transitions used. The S+2W dimension of a line was chosen to match the diameter of the dielectric of the coaxial cable to be attached to it. This choice was made for a smooth mechanical as well as electrical transition. Return and insertion loss measurements were done on two transitions mounted in a back-to-back fashion, in an attempt to isolate the reflection of one transition only. A 50-Ω chip load or a tapered piece of absorber was placed at one end of the CPW and only the return loss measured. Single-frequency measurements were made using the tapered piece of absorber as a sliding load. The vector reflection coefficient was plotted on a Smith chart. The center of the circular locus is a good approximation to the S_{11} of the coax-to-CPW transition, if the magnitude of the transition's S_{22} is small.

The simple arrangement in Figure 7 had several advantages. It was easy to assemble, no machining was required, and semiconductor chips mounted on the flat piece of D-13 would have been easily accessed by a semiconductor bonding machine. Unfortunately, several problems were encountered. Repeated testing flexed the coax cables and eventually broke the epoxy or solder holding them to the D-13. Often some of the metallization would lift off also. The return loss of two back-to-back transitions was not very good; the worst case was a return loss peak of 7 dB at a frequency of 11 GHz. Testing of a low frequency model constructed using 0.125-in. thick Stycast K-12 substrate, copper tape, and large piece of coaxial cable with a type N connector indicated that it was not possible to obtain an acceptable return loss by placing the coaxial cable on top of the substrate and bending the center conductor down to contact the center conductor of the CPW line, as in Figure 7. To obtain a return loss of 15 dB, it was necessary to butt the end of coaxial cable against the edge of the substrate so that the center conductors of the two transmission lines were nearly in the same plane. This is a very reasonable result, considering the field line distributions in the coaxial cable and the CPW.

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5. Wang, N., and Schwarz, S.E. (1982) Planar oscillators for monolithic integration, International Journal of Infrared and Millimeter Waves, 3(No. 6):774-775.

However, this type of connection would be mechanically very weak if attempted using the semi-rigid coaxial cable, epoxy, and solder. A brass test fixture using SMA flange mount connectors was built that allowed the dielectric of the connectors to contact the D-13 in a manner very similar to that in the low-frequency model.

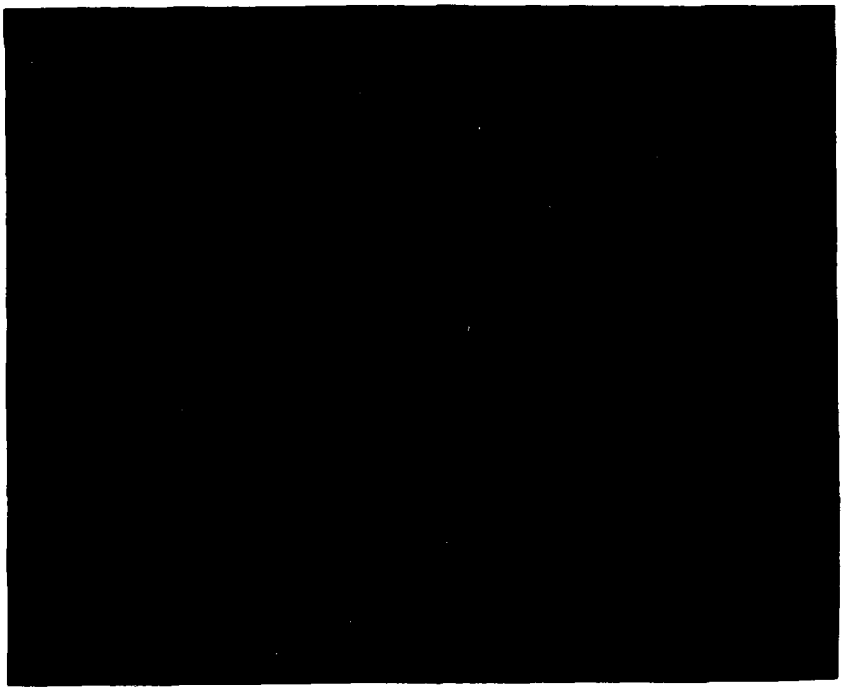

Figure 7. Initial CPW Test Circuit

2.2.2 SMA TEST FIXTURES

Houdart describes a transition from SMA to a CPW line on Alumina using an Omni-Spectra connector, part number 204-8322.[6] A return loss of better than 18 dB up to 12 GHz was claimed for this transition. A diagram, taken from Houdart's paper, of the transition is shown in Figure 8. Clearly visible in Figure 8 are a gap between the substrate and the wall, and two sections of different diameters in the hole through which the dielectric cylinder of the connector passes. SMA test fixtures were built using a close replica of Houdart's transition. Dimensions of the transition that he did not provide were obtained by scaling his diagram from those he did provide. His design was found to perform very poorly; the

6. Houdart, M., and Aury, C. (1982) Various excitation of coplanar waveguide, 1979 MTT-S Symposium Digest, pp. 116-118.

return loss maxima from a test fixture containing a piece of 50-Ω line were at about 7 dB. Eliminating the gap between the substrate and the metal wall, and passing the dielectric of the connector through a simple 0.085-in. diameter hole was found to result in a much better transition. Figure 9 is a plot of the return loss o of a test fixture containing two of these transitions and a straight section of 50-Ω line. This CPW line had S = 0.036 in., W = 0.025 in., and was etched on 0.063-in. thick D-13. Figure 10 shows two of the test fixtures that were designed using the SMA transitions. They are approximately 1-in. long, 0.5-in. wide, and 0.75-in. high.

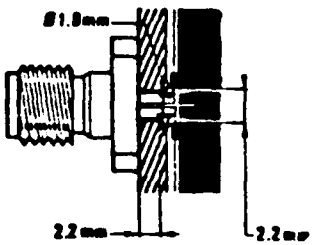

Figure 8. Houdart's SMA Transition to CPW[6]

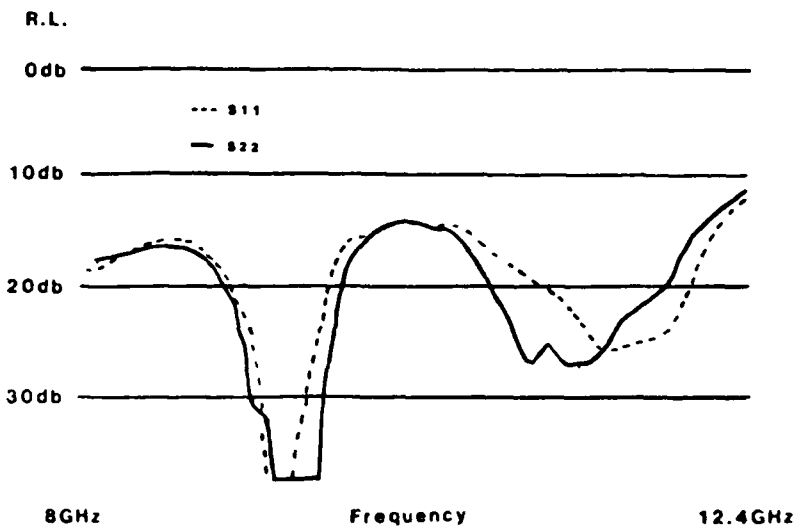

Figure 9. Return Loss of SMA Test Fixture

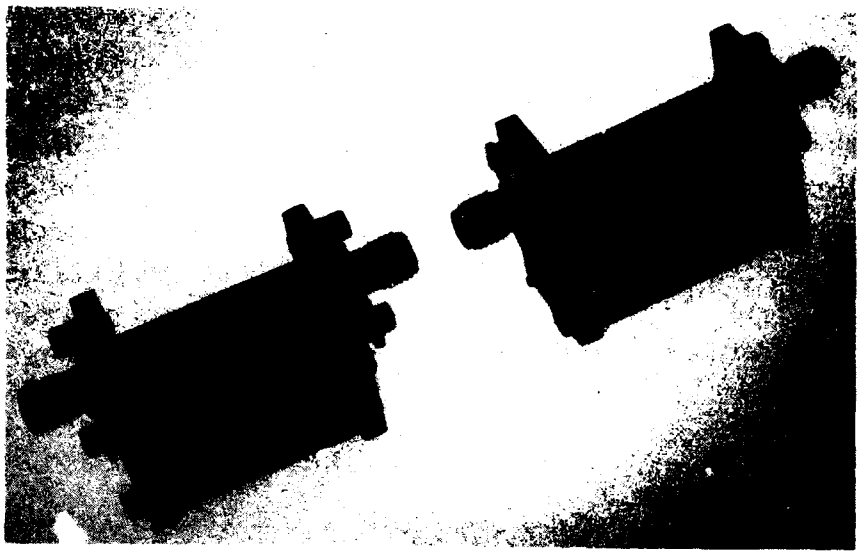

Figure 10. SMA Test Fixtures

It was necessary to mount the substrate up from the bottom block to avoid the excitation of parallel-plate modes in the substrate. The presence of a ground plane on the underside of the substrate changes the CPW to GCPW. A SUPERCOMPACT® analysis revealed that, for the line dimensions mentioned above, the impedance of a GCPW line was not any different than that of CPW line. However, tests made with a ground plane under the bottom of the substrate definitely showed the excitation of modes other than the travelling wave mode. Figure 11 is a plot of the return loss of GCPW on a 0.063-in. thick D-13 substrate mounted in a test fixture using K-connectors in place of the SMA connectors. Touching absorber material to the sides of the substrate would change the return and insertion loss curves noticeably.

To help forestall the excitation of undesired modes in the test fixture, the dimensions of the fixture, including the distance the substrate was raised up from the connecting block, were kept sufficiently small so that the placement of metal walls (copper tape) on the exposed sides of the fixture created a dielectric-loaded waveguide with a cutoff frequency that was above the highest frequency at which the fixture was intended to be used (10 GHz). Testing indicated that this idea did work. The frequency at which the test fixture stopped behaving correctly was pushed to a higher value. Interestingly, a small wire aligned perpendicular to the CPW line and held in the middle of the air gap between the substrate and the bottom of the test fixture had the same effect as the addition of the metal walls.

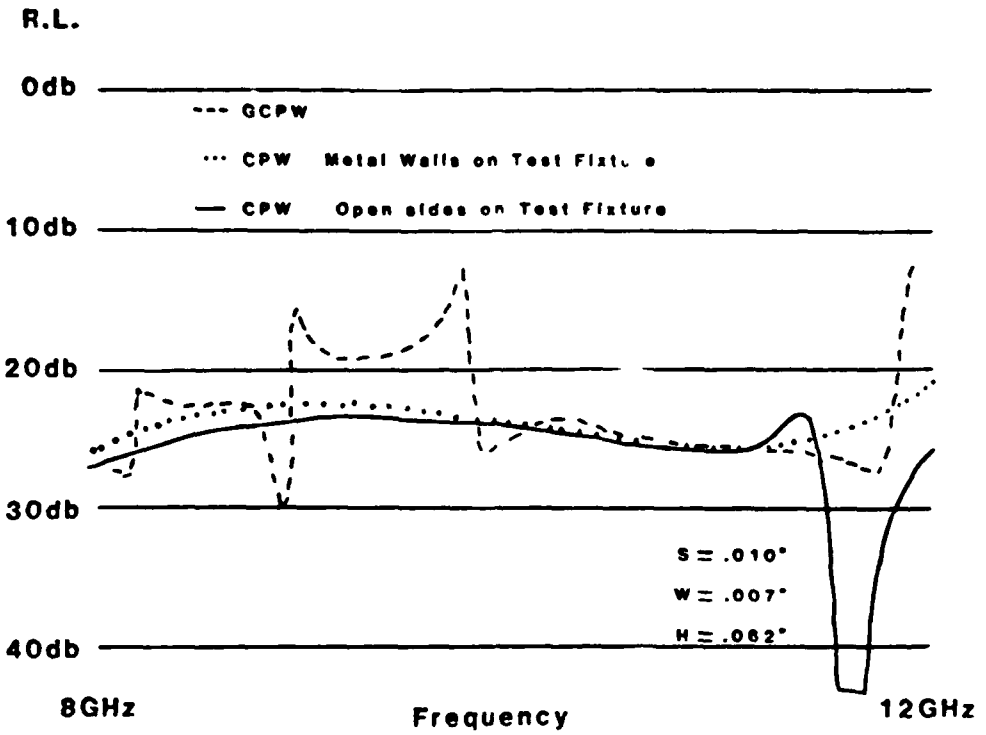

Figure 11. Test Fixture Return Loss, Indicating Existence of Undesired Modes

2.2.3 K-CONNECTOR TEST FIXTURE

A fixture usable to frequencies above 20 GHz was built by replacing the SMA connectors with the female version of the new Wiltron K-connector, and by reducing the substrate thickness from 0.063 in. to 0.025 inch. The 0.025-in. thick substrate was polished to an rms surface roughness of 10 micro-inches to reduce the loss in the CPW lines. The 0.063-in. substrate had been used "as fired." GCPW was tried, but even with the thinner substrate, the return and insertion loss curves indicated the excitation of undesired modes. The substrate was raised to the same height above the ground plane as was used in the SMA test fixtures, and this seemed to be adequate solution. The addition of metal walls was not required. The fixture behaved well up to at least 26 GHz.

A diagram of a K-connector and a photograph of two K-connector fixtures are shown in Figure 12. The K-connector was chosen for a number of reasons. It is compatible with SMA and APC-3.5 type connectors, as well as with other K-connectors, and is capable of single-mode operation up to 46 GHz. The center conductor is mainly supported by a glass bead, as in any airline. Any one connector should be electrically very similar to any other connector, due to tight manufacturing tolerances. This similarity is important, because

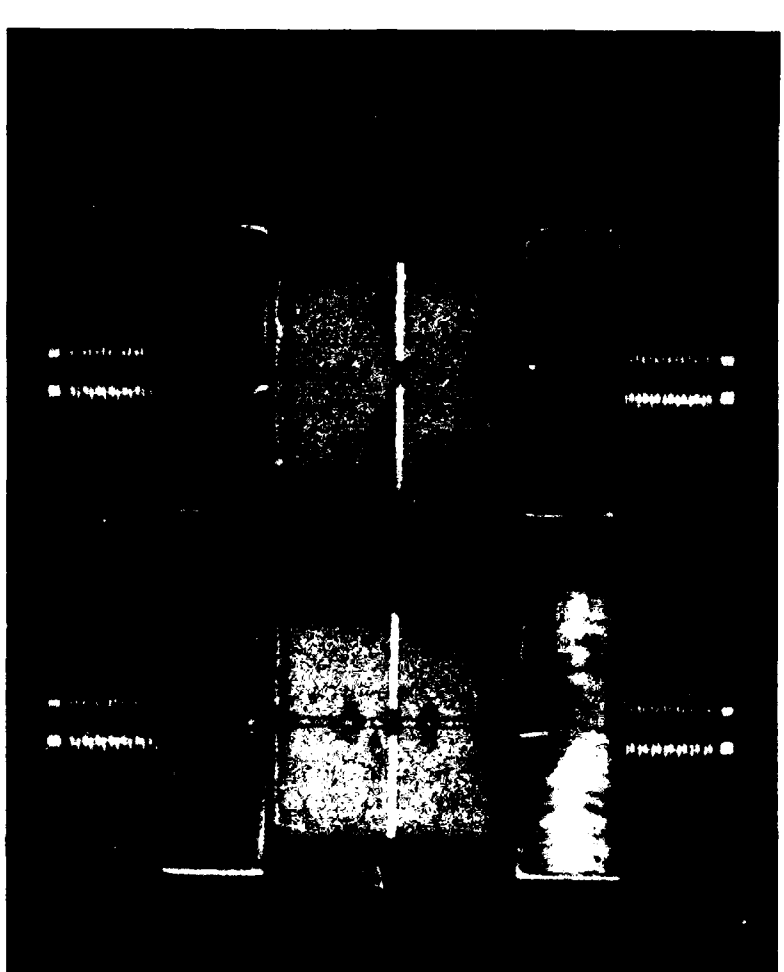

Figure 12. K-connector and K-connector Test Fixtures

the success of the de-embedding routine depends on all the test fixtures containing identical transitions from the outside world to the CPW. The likelihood of several SMA connectors remaining identical to each other as the frequency approached 20 GHz was considered to be remote. (In addition to the fixtures containing the GaAs FET chips to be de-embedded, two other fixtures, each containing a different length of 50-Ω line, were required.) Another benefit that arose from the use of the K-connectors was that a taper in the CPW line was not required. A CPW line with an S+2W dimension of 0.024 in. was optimum both for mounting the Mitsubishi GaAs FET chips and for a smooth physical transition to the K-connector.

Figure 13 is a plot of the return loss of a 50-Ω CPW line of dimensions S = 0.010 in. and W = 0.007 in. mounted in a K-connector fixture. This data was taken using the Wiltron K-connector autotester and a Wiltron 560 scalar network analyzer. Note that the return loss maxima are all below 15 dB, and that $|S_{11}|$ and $|S_{22}|$ very closely track each other, indicating that the transitions on each end of the fixture are indeed electrically very similar. For a lossless fixture, reciprocity would require that $|S_{11}| = |S_{22}|$ for the test fixture even if the transitions were very unlike each other. However, that is not the case here, as there is loss in the CPW lines. Compare Figure 13 with the SMA fixture in Figure 9.

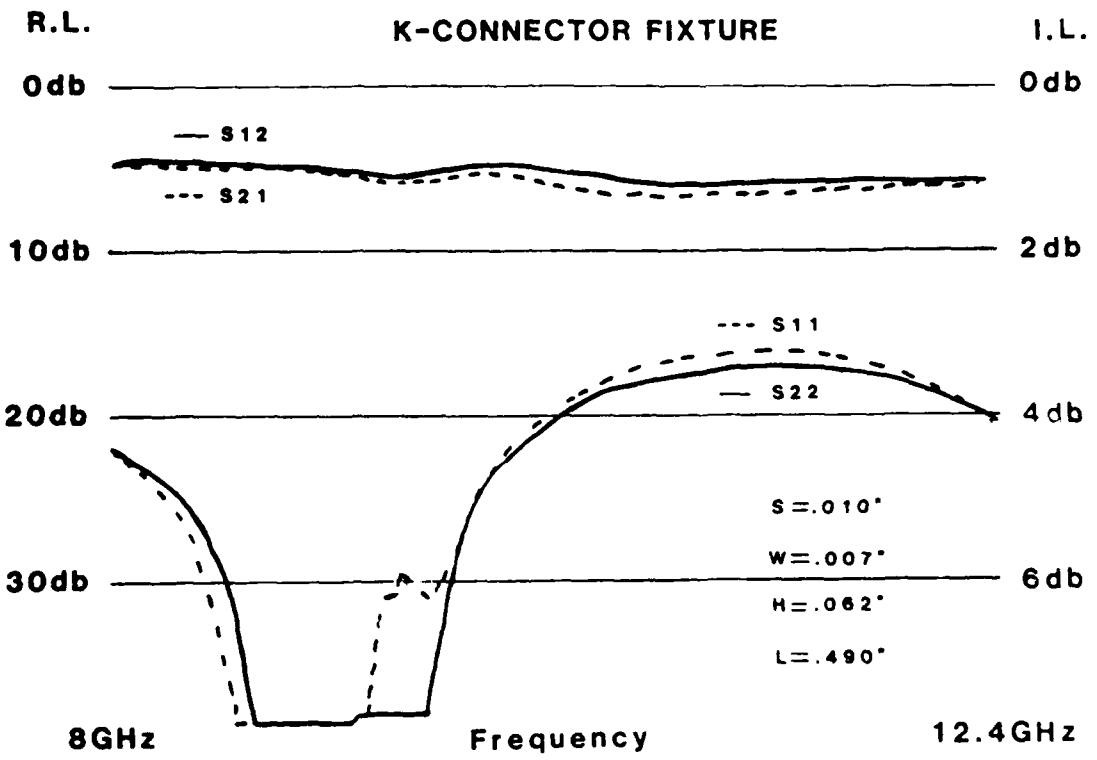

Figure 13. Return and Insertion Loss of K-connector Test Fixtures, as Measured Using a Wiltron K-connector Autotester

In this case $|S_{11}|$ and $|S_{22}|$ do not track very well at all. Figure 14 is a plot of the return and insertion loss of another 50-Ω line mounted in a K-connector test fixture. This data was taken on an Hewlett-Packard (HP) 8510 vector network analyzer. Again, $|S_{11}|$ and $|S_{22}|$ track with each other very well, but note that the return loss is not as good as in Figure 13. The 8510 uses APC-3.5 connectors, and although they do mate with the K-connectors, there is some mismatch due to the different physical dimensions of the two types of connectors. Figure 15 shows

the response of the input CPW to coax transitions of three different test fixtures to the time domain low pass/impulse measurement option on the 8510. This figure indicates that the author did indeed succeed in fabricating identical transitions.

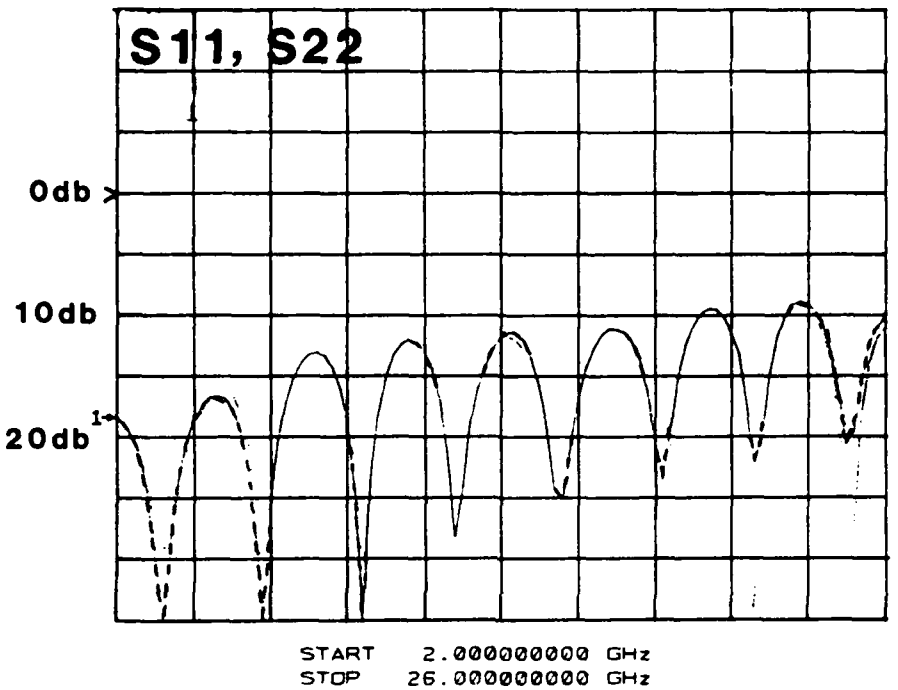

Figure 14. Return and Insertion Loss of K-connector Test Fixtures. Data measured over 2 GHz to 26 GHz frequency range using an HP 8510

All the test fixtures consisted of three pieces—two identical end pieces machined to accept K-connectors and a center block. The end pieces were attached to the block using 4-40 machine screws. The three piece design allowed the length of the test fixture to be adjusted slightly by placing shim material between the end pieces and the block, and this was often necessary to compensate for small differences in the lengths of the D-13 substrates. Kapton film was available in the lab in thicknesses of 0.0005 in., 0.001 in., and 0.005 in., and was found to be suitable as shim material. A large change in the length of a text fixture was made by simply machining a different block. The test fixtures were also designed to allow the bonding machine to access a FET chip mounted on a D-13 substrate in a test fixture. If a chip had to be re-bonded, the test fixture did not have to be disassembled.

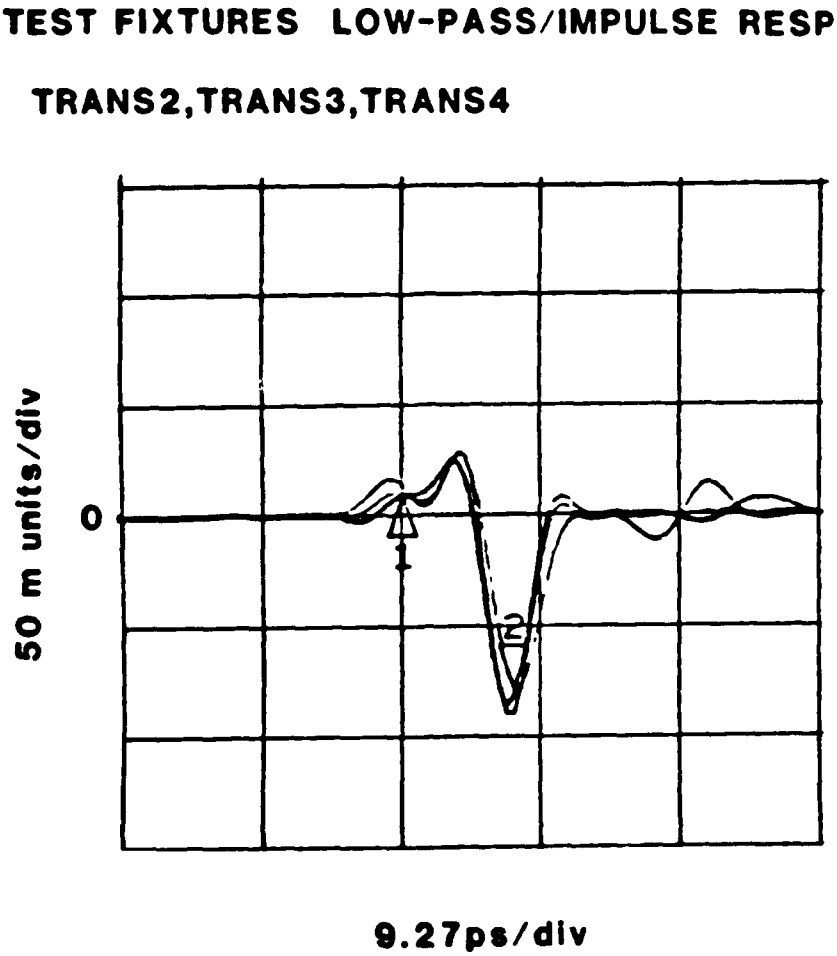

Figure 15. Time-domain Response of Three Separate Transitions From K-connector to 50-Ω CPW Transmission Line

The K-connector fixtures were used to de-embed all the S-parameters used for the design of the 10 GHz and 20 GHz amplifiers, as well as to house all the amplifiers that were constructed.

3. THE DE-EMBEDDING METHOD

The determination of accurate s-parameters of the active devices to be used is a crucial step in the amplifier design process. The design of the amplifier matching networks depends heavily on the s-parameters of the active device. In order for the performance of the final amplifiers to meet the design goals, the s-parameters used in the design must be very close to those of the device used in the amplifier. Unfortunately, it is not practical to measure the actual device to be used in the amplifier.

The active devices used in this project were Mitsubishi 1403 and 1404 GaAs FET chips. For a number of reasons, it was necessary to measure the s-parameters of the FET chips in the lab rather than rely only on those published by the manufacturer. Mitsubishi only provides s-parameters for the 1403 chip to 18 GHz, and the published 1404 s-parameters are for a packaged device, not for a chip. The parasitic reactances associated with the package change the s-parameters noticeably. Also, it is important that the s-parameters are for a FET chip mounted in a configuration that is the same as that used in the final amplifier design. The s-parameters definitely depend on the mounting scheme. The inductance between the source terminal and ground, which affects the maximum available gain obtainable from the FET chip, can be especially sensitive to the mounting arrangement. Mitsubishi's published s-parameters are obtained from chips attached to a metal ridge which separates input and output alumina substrates onto which 50-Ω microstrip lines have been etched. The source bond wires run from the chip down to the metal ridge. The Mitsubishi mounting configuration is very different from the one used to attach the chips in CPW. Finally, the characteristics of GaAs FET chips can be different for each particular lot of devices produced, and the values listed by the manufacturer may be his best rather than representative of an average device.

Figure 16 depicts a FET chip in a test fixture. The first step in de-embedding the s-parameters of the FET chip is to determine the s-parameters of the input and output sections of the test fixture. These s-parameters and those measured for a test fixture containing a FET chip are then all converted to t-parameters and manipulated appropriately using simple matrix math to obtain the t-parameters of the FET chip alone. These t-parameters are next converted back to s-parameters. The whole process is illustrated in Figure 17.

3.1 Characterization of the Embedding Networks

The input and output sections of the test fixture that must be electrically removed in order to determine the FET chip s-parameters are referred to as embedding networks. Several methods have been published for characterizing the embedding networks and de-embedding the s-parameters of a device situated between them. In one of the more commonly used methods, the unterminating procedure, at least three known loads are used to terminate an embedding network.[7] The measured reflection coefficient of the embedding network when it is terminated by a known load would be:

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7. Bauer, R. F., and Penfield, P. (1974) De-embedding and unterminating, IEEE Trans. Microwave Theory Tech., MTT-22(No. 3):282-288.

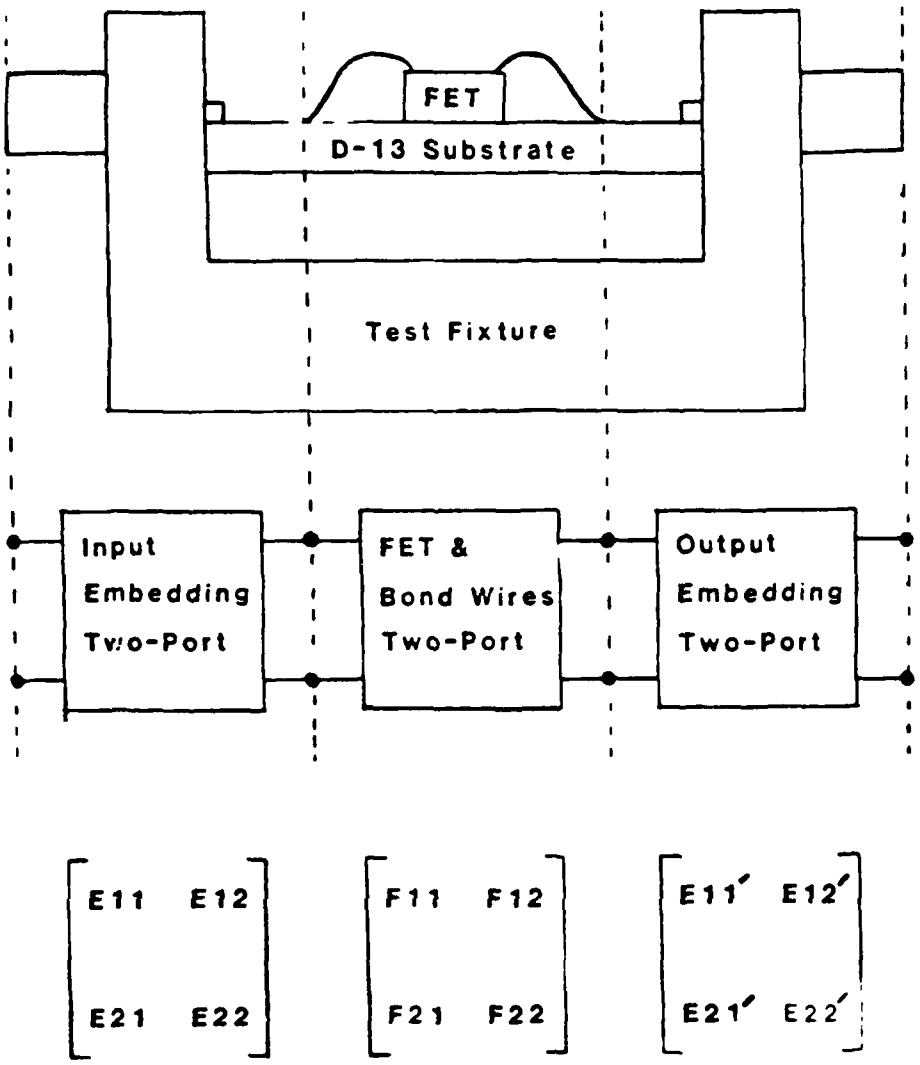


Figure 16. Test Fixture Model Used for De-embedding

$$\Gamma_{Mi} = E_{11} + \frac{(E_{12}E_{21}) \cdot \Gamma_{Li}}{1 - E_{22} \cdot \Gamma_{Li}} \qquad (1)$$

Γ_{Li} = Reflection coefficient of known load i

Γ_{Mi} = Reflection coefficient measured with two-port terminated by known load i.

The s-parameters of the embedding network are referred to as error terms (E_{ij}) to distinguish them from the FET chip s-parameters, that will be referred to as (F_{ij}). Three known loads and the corresponding reflection coefficients measured

$$\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} S11 & S12 \\ S21 & S22 \end{bmatrix} \cdot \begin{bmatrix} a1 \\ a2 \end{bmatrix}$$

TO DE-EMBEDD FET AND BOND WIRES

1 MUST KNOW $\quad [S], [E], [E']$

2 CONVERT ALL TO T-PARAMETERS

$$[S] \triangleright [T], \quad [E] \triangleright [TE], \quad [E'] \triangleright [TE']$$

3 USE MATRIX MATH TO OBTAIN T-PARAMETERS OF FET & BOND WIRES

$$[T] = [TE] \, [TF] \, [TE']$$

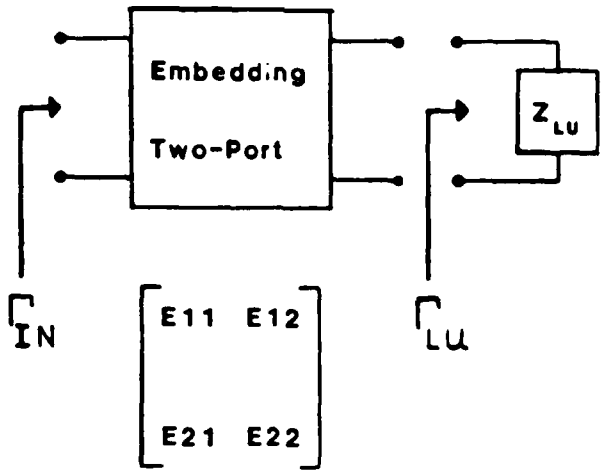
$$[TF] = [TE]^{-1} \cdot [T] \cdot [TE']^{-1}$$

4 CONVERT T-PARAMETERS OF FET & BOND WIRES TO S-PARAMETERS

$$[TF] \triangleright \begin{bmatrix} F11 & F12 \\ F21 & F22 \end{bmatrix}$$

Figure 17. De-embedding Procedure

when each of the known loads is used to terminate the two-port are enough to calculate E_{11}, E_{22}, and the product $E_{12}E_{21}$. Suppose, for example, that it was now desired to de-embed the reflection coefficient of a one-port that was cascaded with the two-port embedding network just characterized, as in Figure 18. A rearrangement of the bi-linear transform yields



$$E11 = F_1(\Gamma_{M1}, \Gamma_{M2}, \Gamma_{M3}, \Gamma_{L1}, \Gamma_{L2}, \Gamma_{L3})$$

$$E22 = F_2(\Gamma_{M1}, \Gamma_{M2}, \Gamma_{M3}, \Gamma_{L1}, \Gamma_{L2}, \Gamma_{L3})$$

$$(E12E21) = F_3(\Gamma_{M1}, \Gamma_{M2}, \Gamma_{M3}, \Gamma_{L1}, \Gamma_{L2}, \Gamma_{L3})$$

Γ_{Mi} = Reflection Coefficient of Two-Port When Terminated With Known Load

Γ_{Li} = Reflection Coefficient of Known Load i

Γ_{Lu} = Reflection Coefficient of Unknown Load

Figure 18. De-embedding a One-port by the Unterminating Method

$$\Gamma_{Lu} = \frac{\Gamma_{in} - E_{11}}{(\Gamma_{in} E_{22} + E_{12} E_{21} - E_{11} E_{22})} \qquad (2)$$

Note that only the product $E_{12} E_{21}$ is required to de-embed Γ_{Lu}. If a two-port was flanked by two embedding networks of equal error terms, it is not necessary to break this product to de-embed all the s-parameters of the two-port. Reciprocity requires $E_{12} = E_{21}$, or $E_{12} = E_{21} = \sqrt{E_{12} E_{21}}$. If the value of E_{12} or E_{21} is needed, some general knowledge of the embedding network can be used to resolve the sign ambiguity in taking the square root.

The unterminating method can be implemented in a number of different ways. The known loads can be placed in the actual text fixture used for the FET chip, and used to terminate first the input embedding network and then the output embedding network. Another possibility is to build three separate half fixtures, each terminated with a different known load, and to assume that the input embedding network, the output embedding network, and all of the half fixtures are electrically equal. The three half fixtures are used to obtain the error terms, and these are then used to de-embed an active device mounted in a test fixture.

Although three is the minimum number of loads that is required to characterize an embedding network, the use of more loads and a minimization routine can provide more accuracy if there is error in the data or loads. This is discussed in the paper on unterminating.[7] Glasser[8] has derived bounds on the maximum error involved in de-embedding the reflection coefficient of a one-port when the embedding network has been characterized using three known loads in the unterminating procedure.[8] Sources of error he considered were uncertainty in the knowledge of the "known" loads and uncertainty in all the measurements required. Error was defined as the magnitude of the difference vector between the de-embedded reflection coefficient and the true reflection coefficient of the embedded one-port. His analysis indicated that the bounds on the error are largest when the reflection coefficient of the one-port being de-embedded is located in an area of the Smith chart that is remote from the locations of the reflection coefficients of the loads used for unterminating. In an example he presented, a short, open, and load were used as the known loads. The bound on the de-embedding error was three times as large when de-embedding a one-port reflection coefficient of $1\angle 90°$ than for de-embedding a one-port whose reflection coefficient was closer to that of one of the known loads.

The unterminating procedure was not used in this project to characterize the FET chip's embedding networks. At the time, the author doubted that he could create loads in CPW whose value could be reliably known up to a frequency of 20 GHz. A method published by Souza[9] was modified and used instead. It was chosen because it was relatively simple and does not require known loads to characterize the embedding networks. The loads were thus eliminated as a possible source of error. Two test fixtures containing different lengths of 50-Ω line are used to characterize the embedding networks. Required as "knowns" are the guide wavelength, the impedance of the CPW line, and the difference in length between the two 50-Ω lines. This difference is referred to as $\Delta\ell$. The analysis assumes that each test fixture

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8. Glasser, L.A. (1978) An analysis of microwave de-embedding errors, IEEE Trans. Microwave Theory Tech., MTT-26(No. 5):379-380.

9. Souza, J.R., and Talboys, E.C. (1982) S-parameter characterization of coaxial to microstrip transition, IEEE Proceedings, 129(No. 1).

consists of two electrically equal half fixtures connected in the back-to-back fashion. The fixture with the shorter piece of 50-Ω line is referred to as THRUS, and the fixture with the longer piece is referred to as THRUL. THRUS is considered to be made up of two half fixtures directly connected to each other, and THRUL to consist of two half fixtures separated by a piece of 50-Ω line ($\Delta \ell$). A test fixture with a FET chip has a half fixture attached to the input of the FET chip, and another cascaded with the output of the chip. The idea is illustrated in Figure 19. Any half fixture from any test fixture is considered interchangeable with any half fixture from any other test fixture. This assumption simplifies the analysis considerably, and great care was exercised in assembling the test fixtures to ensure that they were all the same.

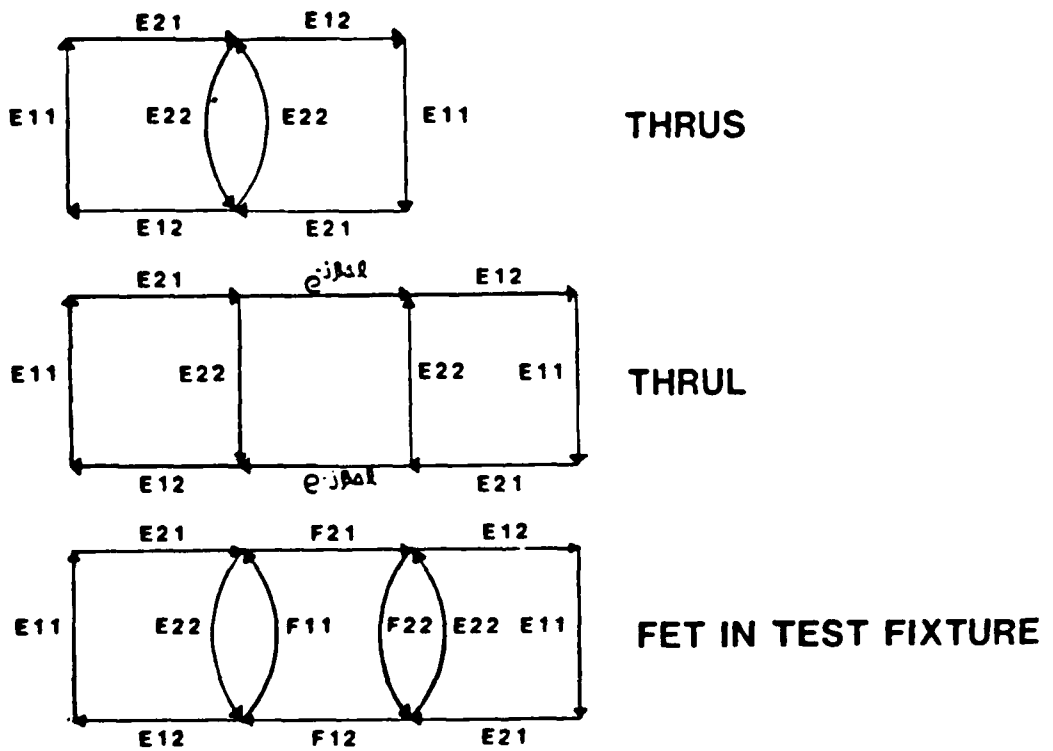


Figure 19. Flow Graphs of De-embedding Test Fixtures

The equations for characterizing the embedding networks using this method are easily derived. The s-parameters of THRUS and THRUL are measured using a previously calibrated network analyzer. Three of these s-parameters are necessary. The input reflection coefficient of THRUS, Γ_0, the input reflection coefficient of THRUL, $\Gamma_{\Delta \ell}$, and the transmission coefficient of THRUS, T_0. The use of the bilinear transformation yields:

$$\Gamma_0 = E_{11} + \frac{(E_{12}E_{21})E_{22}}{1 - (E_{22})^2} \tag{3}$$

$$\Gamma_{\Delta\ell} = E_{11} + \frac{(E_{12}E_{21})E_{22}\, e^{-2j\beta\Delta\ell}}{1 - (E_{22})^2\, e^{-2j\beta\Delta\ell}} \tag{4}$$

T_0 can be found by considering multiple reflections and using the formula for the geometric progression. It yields:

$$T_0 = \frac{(E_{21}E_{12})}{1 - (E_{22})^2} \tag{5}$$

If the transition from the test fixture connector to the CPW is good, then $E_{22}^2 << 1$ and the equations can be simplified to:

$$\Gamma_0 = E_{11} + (E_{12}E_{21})E_{22} \tag{6}$$

$$\Gamma_{\Delta\ell} = E_{11} + (E_{12}E_{21})E_{22} \cdot e^{-2j\beta\Delta\ell} \tag{7}$$

$$T_0 = (E_{12}E_{21}) . \tag{8}$$

These three equations contain three unknowns and are easily solved to give:

$$E_{11} = \frac{\Gamma_{\Delta\ell} \cdot e^{+j\beta\Delta\ell} - \Gamma_0 \cdot e^{-j\beta\Delta\ell}}{2j \sin(\beta\Delta\ell)} \tag{9}$$

$$E_{22} = \frac{j(\Gamma_{\Delta\ell} - \Gamma_0)\, e^{+j\beta\Delta\ell}}{2T_0 \sin(\beta\Delta\ell)} \tag{10}$$

$$E_{12}E_{21} = T_0 . \tag{11}$$

These are the equations presented in Reference 9. The authors, however, only used the method derived here to frequencies of 4 GHz. At 20 GHz, the assumption that $E_{22}^2 << 1$, even for carefully constructed test fixtures, may not be valid. A more exact solution was obtained by using the values of E_{11}, E_{22}, and $E_{12}E_{21}$ calculated from the equations above as starting values in an iterative procedure using exact expressions derived without neglecting E_{22}^2. These more exact expressions are:

$$E_{11} = \frac{\Gamma_{\Delta\ell}\, e^{+j\beta\Delta\ell}\,(1 - E_{22}^2\, e^{-2j\beta\Delta\ell}) - \Gamma_0(1 - E_{22}^2)\, e^{-j\beta\Delta\ell}}{2j \sin(\beta\Delta\ell)} \tag{12}$$

$$E_{22} = \frac{j\, e^{+j\beta\Delta\ell}\quad \left[(1 - E_{22}^2\, e^{-2j\beta\Delta\ell})\,\Gamma_{\Delta\ell} - (1 - E_{22}^2)\Gamma_0\right]}{2j \sin(\beta\Delta\ell)\quad \left[E_{12}E_{21} - E_{11}E_{22}\right]} \tag{13}$$

$$E_{12}E_{21} = T_0\,(1 - E_{22}^2) \tag{14}$$

If E_{22}^2 is ignored, the above expressions can be shown to simplify to the previous equations. A computer program was written to perform the iterative procedure. The computer would compute E_{ij} in each of the above expressions, insert the new value of E_{22} calculated from the second equation into all expressions, and recompute them. The procedure was terminated when the magnitude of the difference between consecutive values of each of the error terms was less than a preset value (usually 0.005). This iterative procedure worked well, and convergence always occurred, except when data grossly in error was fed into the computer. The s-parameters used to design 10 GHz and 20 GHz amplifiers were all obtained in this manner.

3.2 Obtaining Device S-Parameters

The procedure used to obtain s-parameters of a FET chip once its embedding networks have been characterized was mentioned briefly and outlined in Figure 17. The equations are easily derived from the use of s-parameters and t-parameters, and are presented in Figure 20. The s-parameters of the FET chip are referred to as F_{ij}, and the s-parameters measured when the FET chip is in a test fixture are referred to as S_{ij}. The t-parameters of the FET chip were calculated first, and are referred to as TF_{ij}.

All the equations necessary to de-embed the FET chip's s-parameters were programmed in FORTRAN on a VAX™ 11/750 computer. A program called DMBED.FOR performed the iterative procedure to calculate the embedding network error terms. A separate program, FTDMBED.FOR, used the error terms and the s-parameters of a FET chip in a test fixture to produce the s-parameters of the FET chip alone. The actual de-embedded s-parameters of 1403 and 1404 FET chips and the details of the measurement procedure are discussed in Section 3.3.

$$TF11 = \frac{-E_{11}^{2} + (S_{11} + S_{22})\,E_{11} - \Delta S}{(E_{12}\,E_{21})\,S_{21}}$$

$$TF12 = \frac{(E_{11} - S_{11})\,\Delta E + E_{22}\,(\Delta S - S_{22}\,E_{11})}{(E_{12}\,E_{21})\,S_{21}}$$

$$TF21 = \frac{(S_{22} - E_{11})\,\Delta E + E_{22}\,(E_{11}\,S_{11} - \Delta S)}{(E_{12}\,E_{21})\,S_{21}}$$

$$TF22 = \frac{(\Delta E)^{2} - E_{22}\,(S_{11} + S_{22})\,\Delta E + E_{22}^{2}\,\Delta S}{(E_{12}\,E_{21})\,S_{21}}$$

$$F11 = TF12/TF22 \qquad F12 = \frac{\Delta TF}{TF22}$$

$$F21 = 1/TF22 \qquad F22 = -TF21/TF22$$

WHERE: $\Delta A = A11 \cdot A22 - A12 \cdot A21$

Figure 20. De-embedding equations

3.3 Test of Error

The de-embedding method was tested, using the computer, to gain a qualitative idea of the magnitude of error possible in the de-embedded s-parameters. Models created on SUPERCOMPACT® of THRUS, THRUL, and a typical FET chip in a test fixture were used to generate the input data for DMBED.FOR and FTDMBED.FOR. A parallel capacitor was used to model the K-connector-to-CPW transition in each test fixture. The s-parameters of typical FET chips were created by using SUPERCOMPACT® to extrapolate to 26 GHz the values listed on the Mitsubishi 1403 chip data sheet. The de-embedded s-parameters and the s-parameters of the typical FET were then plotted and compared. Initially, before any de-embedding was tried with any FET chips in the lab, the models were used to determine if the iterative procedure always converged to sufficiently accurate values of the error terms. Even when THRUS and THRUL models whose return loss maxima were

5 dB were used, the iterative procedure converged and the de-embedded s-parameters were correct.

Often, however, later attempts to de-embed FET chips using data measured on an HP 8409 or HP 8510 network analyzer would generate de-embedded s-parameters that seemed to bear little resemblance to those that should be characteristic of any real active device. The de-embedding method was again tested on the computer, this time to determine if any extreme sensitivities existed to input or other error that could be responsible for the strange output, such as that in Figure 21, that was occasionally obtained. There are several avenues by which error could enter the de-embedding procedure. The possibilities include uncertainty in the measurement of Γ_0, $\Gamma_{\Delta\ell}$, and T_0, uncertainty the measurement of $\Delta\ell$, and any uncertainty in the knowledge of the Keff or ZO of the CPW line. Also, the assumption that all the embedding networks have equal error term matrices would be violated, if, for example, the K-connector-to-CPW transitions in THRUS were any different than the transitions in one of the other fixtures. This would introduce error into the final de-embedded s-parameters. The DMBED.FOR program was modified to include the effects of loss in $\Delta\ell$, eliminating this as a source of error.

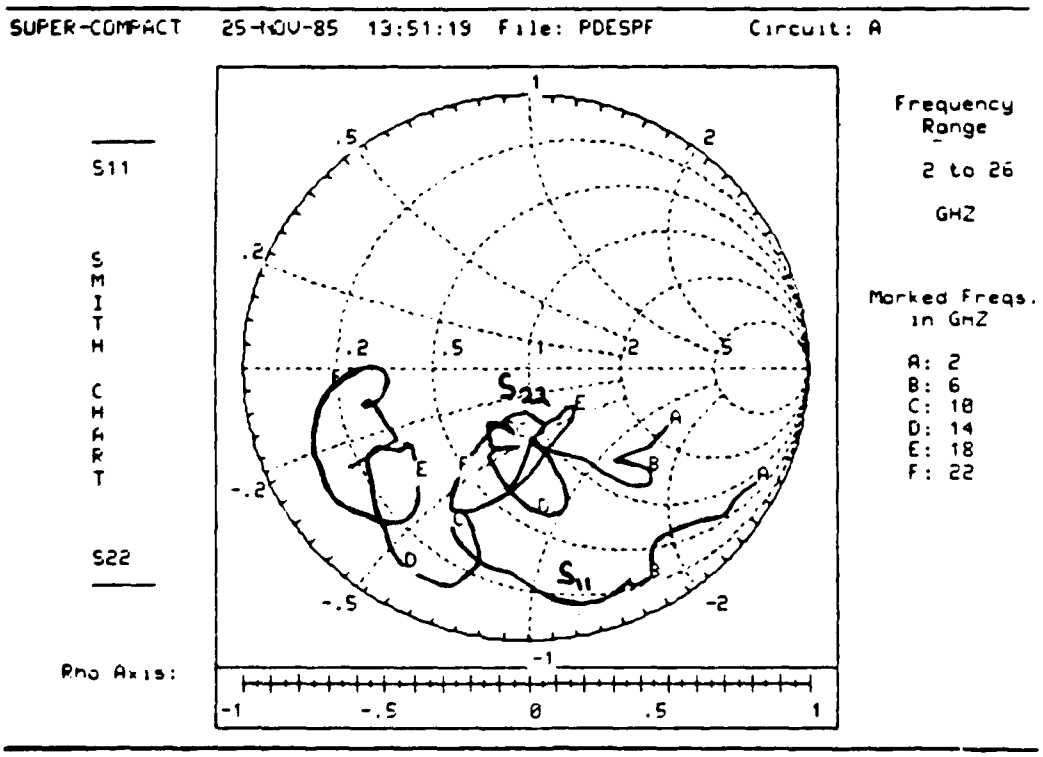


Figure 21. De-embedded s-parameters Occasionally Obtained

Relative to the error displayed in Figure 21, tests on the computer using the models on SUPERCOMPACT® showed the de-embedding method to be rather insensitive to small errors in the input data or to small discrepancies in the error terms of the embedding networks. Most output such as that in Figure 21 was found to be due to gross errors in the measured data stemming from bad calibration procedures, the use of damaged adapters, or from a poorly assembled test fixture.

The magnitude of error the computer modeling did generate in the de-embedded s-parameters is displayed in Figure 22. Figure 22 shows the typical s-parameters, that should correspond to the de-embedded s-parameters if there is no error, the de-embedded S_{11} and S_{22} obtained when there is an asymmetry in the test fixtures, and the de-embedded S_{11} and S_{22} obtained when the data for each test fixtures is taken at a different frequency. To model an asymmetry a 0.070-in. length of 50-Ω air line was added to the output half of each of the test fixtures, corresponding to a 55° phase difference between the S_{11} and S_{22} of THRUS or between the S_{11} and S_{22} of THRUL at 26 GHz. This is a large phase asymmetry, but the resulting de-embedded s-parameters still bear a fair resemblance to the correct s-parameters. The curve labeled frequency error was generated by using a relative shift in the frequencies at which the models were analyzed. The THRUS data was for a frequency 200 MHz below that of the THRUL data, and is 100 MHz below that of the test fixture with the typical FET chip in it. This frequency shift is well outside the range of the possible frequency error of an HP sweeper, but it served to test the effect of small errors in Γ_0, $\Gamma_{\Delta\ell}$, and T_0 on the de-embedded s-parameters. A test was also performed to determine the effect of dispersion in the CPW transmission lines on the de-embedded s-parameters. Microstrip with a Keff that ranged from 8.2 at 2 GHz to 9.5 at 26 GHz was used in all the SUPERCOMPACT® models of the test fixtures, while only the low frequency Keff value was used to calculate the electrical length of $\Delta\ell$ in DMBED.FOR. The de-embedded s-parameters showed the same trend as those in Figure 22—error certainly existed but it was not catastrophic. In all the above cases, the models used physical lengths of transmission line and values of Keff that closely corresponded to those of actual test fixtures.

3.4 Error Correction and De-embedding

The error correction procedure used to enhance the accuracy of automatic network analyzers is almost exactly the same as the procedure to de-embed a two-port network from embedding networks connected to its input and output. In the forward and reverse transmission error models used in a full 12-term error correction process on an HP 8510 network analyzer, the DUT is essentially a two-port sandwiched between input and output embedding networks. The error terms in

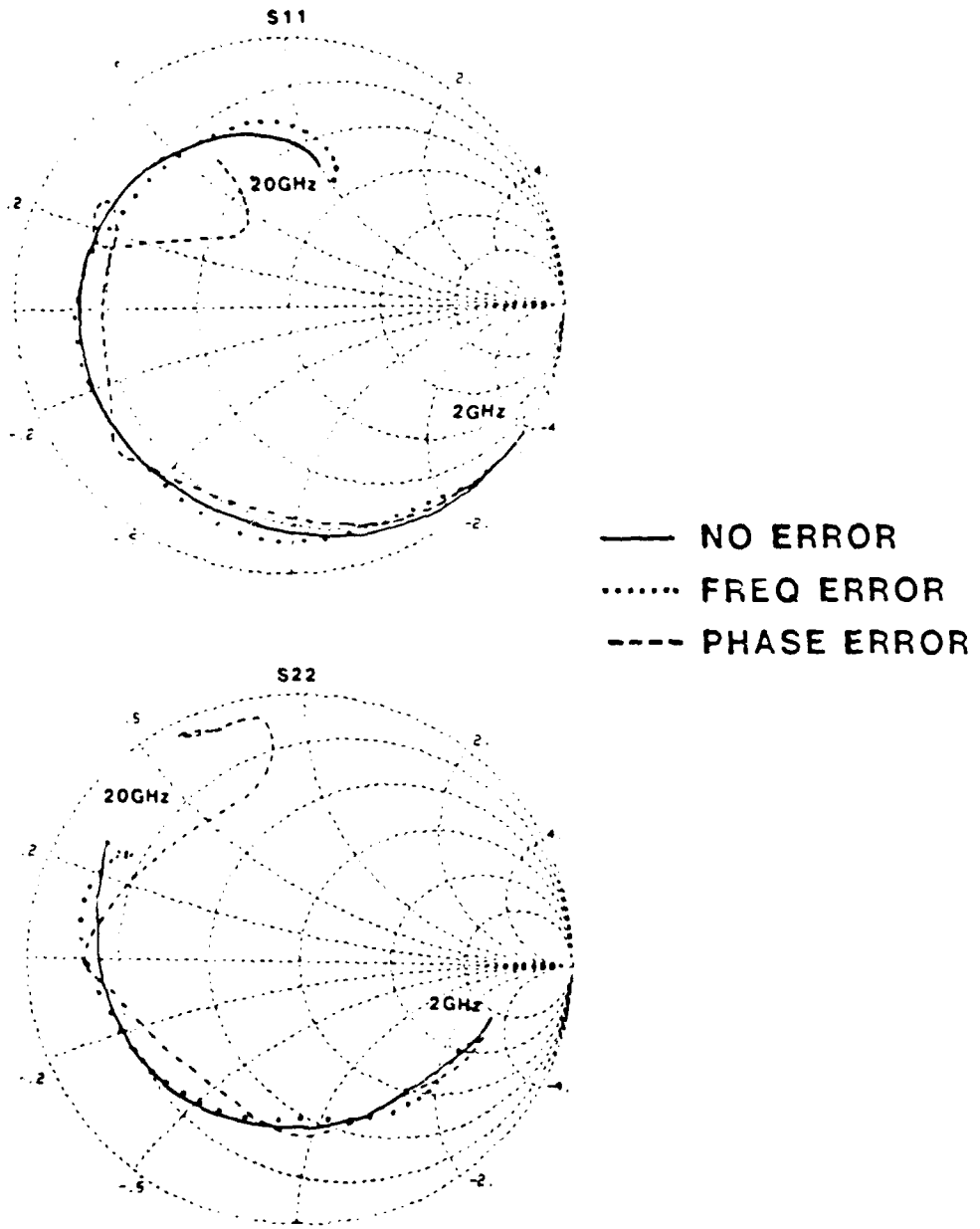


Figure 22. Test of Error

the model arise from sources internal to the network analyzer, such as the directivity of the couplers or bridges, and the through-loss and mismatch of the other various components in the signal path. Twelve terms are used in the error correction process because different measurement hardware is switched into the signal path for forward transmission measurements than for reverse transmission measurements, and a correction for internal cross-talk is also included.

In this project, the network analyzer error terms were determined through the use of calibration standards supplied by HP, and measurements made, using the calibrated network analyzer, of the THRUS and THRUL fixtures were used to determine the error terms of the test fixtures. This method is referred to as two-tier de-embedding. If one is willing to extend the equal error term assumption to the network analyzer also, one set of error terms representing the network analyzer and the test fixtures can be calculated based on uncorrected measurements of THRUS and THRUL. The network analyzer would then directly display the de-embedded s-parameters of an FET chip when a FET chip in a test fixture was connected as the DUT. This approach is referred to as one-tier de-embedding. In the case of the THRUS and THRUL de-embedding method, the one-tier technique is probably less accurate than the two-tier technique because it requires the equal-error term assumption to be applied to the network analyzer. However, in the case of the unterminating procedure, the one-tier approach still allows the input and output error terms to be calculated separately. For example, the necessary measurements can be made by independently attaching half-fixtures, each containing a different known load, to port 1 and port 2 of the network analyzer, and then attaching a through fixture containing a 50-Ω line between port 1 and port 2. The error terms calculated by the network analyzer now include the effects of the test fixture halves. If the reflection coefficient of the load in each half-fixtures is known fairly well, the one-tier approach can probably save time over the two-tier approach, without unduly compromising accuracy.

3.5 De-embedding Measurement Technique

The data for the 10 GHz de-embedding effort were taken on an HP 8409 network analyzer that used an eight-term error correction model. The eight-term error model corrects reflection and transmission measurements for source mismatch but not for load mismatch. A 12-term model, such as that programmed on the HP 8510, corrects all s-parameters for source and load mismatches and also includes a cross-talk correction. The 20 GHz de-embedded s-parameters were calculated from data taken on an HP 8510 network analyzer. In both the 10 GHz and 20 GHz de-embedding efforts, a piece of 50-Ω CPW line was de-embedded to test the measured data and the computer programs. If the data was taken on the HP 8510, the de-embedded S_{21} of the line was always less than zero, however, if the HP 8409 was used to measure the fixtures, the de-embedded S_{21} of a 50-Ω line would often show a "gain" of a few tenths of a dB. Obviously, the more sophisticated error model does yield better results.

In order to calibrate the network analyzer, it is necessary to connect port 1 to port 2. If sexed connectors are being used, then port 1 and port 2 must terminate in connectors of the opposite sex. This presents a problem when attempting to measure, after calibration, a two-port device that has the same sex connectors on each port. Adding an adapter to the system will invalidate the error terms calculated during the calibration process. A device that has the same sex connectors on each port is known as "non-insertable." The K-connector test fixtures, with female connectors on each port, fall into this category. Unfortunately, sexless connectors such as the APC-7 are only good to 18 GHz. A test fixture with a male K-connector on one end and a female K-connector on the other would have been ideal for measurement purposes, but would have violated the equal embedding network assumption used in the de-embedding routine.

An HP technical note has been published that describes methods by which non-insertable devices can be measured.[10] The usual method employed is called the "switched-adapter" technique. If, for example, both ports of the network analyzer are terminated in APC-7 connectors, and a device terminated in SMA connectors is to be measured, then APC-7 to SMA adapters must be placed on the measurement ports of the network analyzer. If an APC-7 to female SMA adapter is placed on port 1, an APC-7 to SMA male connector is placed on port 2 for calibration purposes. To measure a two-port device terminated on both ends with male connectors, the APC-7 to SMA male adapter on port 2 is replaced with an APC-7 to female SMA adapter. The adapters are assumed to be electrically equal. Strictly speaking, the calibration is invalidated, but hopefully, only to a small degree. There is another method, called "special calibration C" in the HP technical note, that can be used to exactly measure non-insertable devices. It requires a more involved calibration procedure, but this can be programmed into the HP network analyzer's error correction routine.

The "switched-adapter" technique was used to take the data necessary to de-embed the 20 GHz s-parameters. A superfluous APC-3.5 male-to-female adapter was included when calibrating the HP 8510, and then replaced with a male-to-male adapter in order to take measurements. It seemed to work well. In the case of the 10 GHz FET s-parameters, the fixtures were made insertable and their symmetry was maintained by placing APC-7 to SMA male adapters on each end of the fixture. The network analyzer was calibrated in APC-7 connectors.

The use of automated procedures greatly helped in obtaining the de-embedded s-parameters of the 1403 and 1404 GaAs FET chips, and in measuring the 10 GHz

10. Fitzpatrick, J., and Williams, J. (1981) Measuring non-insertable devices with an ANA, Hewlett-Packard technical reprint 5952-9326 from Microwave System News.

and 20 GHz amplifiers. Specifically, measurement data taken on both the 8409 and 8510 network analyzers was written directly into data files on a VAX™ 11/730 computer. In using the 8510, the data did have to be recorded on cassette tapes as an intermediate step, but the extra time involved was minimal.

4. DE-EMBEDDED S-PARAMETERS OF FET CHIPS

In the previous section, the de-embedding method was presented. This section discusses the de-embedded s-parameters used to design the 10 GHz and 20 GHz amplifiers and the arrangement used to mount the FET chip to the D-13 substrate. The use of the de-embedding method to obtain an approximation of the loss in the CPW lines is also considered.

Two methods were tried for mounting the FET into the D-13 substrate material. Because the amplifiers designed for this project were intended to provide information on the feasibility of monolithic amplifiers, it was decided to mount the FET chip into, rather than on top of, the substrate. This arrangement would provide a better model of a monolithic environment. The two mounting methods tried are described in this section.

4.1 Mitsubishi Data

Full data sheets for the 1403 and 1404 GaAs FET devices are readily available from Mitsubishi. Mitsubishi's s-parameters for the 1403 chip are listed in Table 1 for drain-to-source (Ids) current levels of 10 mA and 30 mA. In Figures 23a and 23b, the s-parameters corresponding to an Ids of 30 mA are plotted. Mitsubishi recommends the lower Ids for low-noise applications, and the higher Ids for high-gain applications. Despite repeated requests, Mitsubishi only supplied data for the packaged 1404 FET chip, and these s-parameters are not representative of those of a discrete chip, due to parasitic reactances associated with the package. The 1404 packaged chip data can also be obtained from Mitsubishi, and they are not listed or plotted here.

As previously emphasized, the s-parameters of a GaAs FET chip depend on the manner in which it is mounted into the circuit. The s-parameters from the data sheets cannot be expected to agree exactly with the de-embedded s-parameters. Nevertheless, a comparison was often useful, especially for quantities calculated from the s-parameters, such as Maximum Available Gain (MAG), at least to verify that the de-embedding scheme was not in gross error.

Table 1. Mitsubishi Data Sheet 1403 s-parameters and MSG

CIRCUIT: IDS10
S-MATRIX, ZS = 50.0+J 0.0 ZL = 50.0+J 0.0

Ids=10mA

Freq	S11		S21		S12		S22		S21
GHZ	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang	dB
2.00000	0.975	-30.3	2.600	154.5	0.041	70.3	0.761	-16.1	8.30
4.00000	0.949	-48.2	2.290	132.2	0.063	60.1	0.727	-25.0	7.20
6.00000	0.919	-68.6	2.060	116.3	0.075	49.2	0.695	-34.1	6.23
8.00000	0.847	-96.3	1.910	96.3	0.066	34.4	0.673	-45.0	5.62
10.00000	0.814	-120.9	1.800	76.0	0.056	50.1	0.670	-61.8	5.11
12.00000	0.798	-146.4	1.710	56.3	0.075	63.0	0.664	-82.3	4.66
14.00000	0.786	-171.0	1.580	29.1	0.105	34.6	0.665	-105.6	3.97
16.00000	0.771	165.1	1.380	3.1	0.110	49.3	0.710	-131.7	2.80
18.00000	0.745	137.5	1.250	-36.3	0.175	32.1	0.730	-161.9	1.91

CIRCUIT: IDS30
S-MATRIX, ZS = 50.0+J 0.0 ZL = 50.0+J 0.0

Ids=30mA

Freq	S11		S21		S12		S22		S21
GHZ	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang	dB
2.00000	0.970	-33.2	3.310	153.5	0.034	71.5	0.733	-16.0	10.40
4.00000	0.937	-54.0	2.900	130.3	0.053	64.3	0.699	-24.7	9.25
6.00000	0.881	-76.8	2.670	114.0	0.067	56.5	0.667	-33.1	8.53
8.00000	0.815	-102.2	2.480	94.1	0.070	43.2	0.639	-43.8	7.89
10.00000	0.783	-125.9	2.280	74.3	0.050	50.2	0.633	-60.3	7.16
12.00000	0.778	-152.1	2.080	54.0	0.066	67.6	0.630	-80.5	6.39
14.00000	0.768	-177.1	1.930	32.1	0.119	14.0	0.635	-103.6	5.71
16.00000	0.753	157.3	1.730	1.2	0.080	57.1	0.675	-129.1	4.76
18.00000	0.709	128.1	1.560	-38.6	0.153	32.3	0.709	-159.3	3.86

CIRCUIT: IDS10

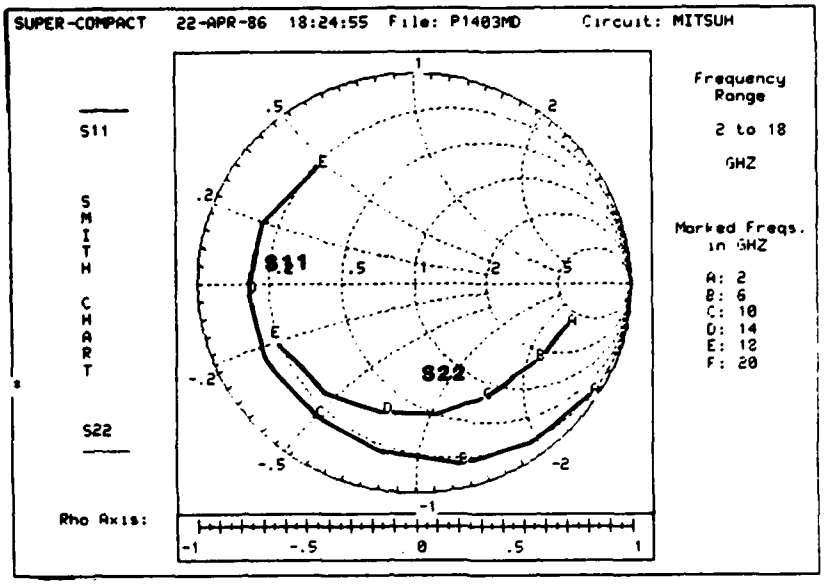
Ids=10mA

Freq	K	SIGN	*--- MAX GAIN ---* AVAILABLE	STABLE	*---- CONJUGATE MATCH GAMMA ---* SOURCE		LOAD	
GHZ		B1	dB	dB	Mag	Ang	Mag	Ang
2.00000	0.135	+		18.02				
4.00000	0.289	+		15.80				
6.00000	0.357	+		14.39				
8.00000	0.656	+		14.61				
10.00000	0.631	+		15.07				
12.00000	0.338	+		13.58				
14.00000	0.233	+		11.77				
16.00000	0.221	+		10.98				
18.00000	0.074	+		8.54				

CIRCUIT: IDS30

Ids=30mA

Freq	K	SIGN	*--- MAX GAIN ---* AVAILABLE	STABLE	*---- CONJUGATE MATCH GAMMA ---* SOURCE		LOAD	
GHZ		B1	dB	dB	Mag	Ang	Mag	Ang
2.00000	0.138	+		19.33				
4.00000	0.242	+		17.38				
6.00000	0.331	+		16.00				
8.00000	0.539	+		15.49				
10.00000	0.751	+		16.59				
12.00000	0.448	+		14.99				
14.00000	0.165	+		12.10				
16.00000	0.116	+		13.09				
18.00000	0.202	+		10.95				



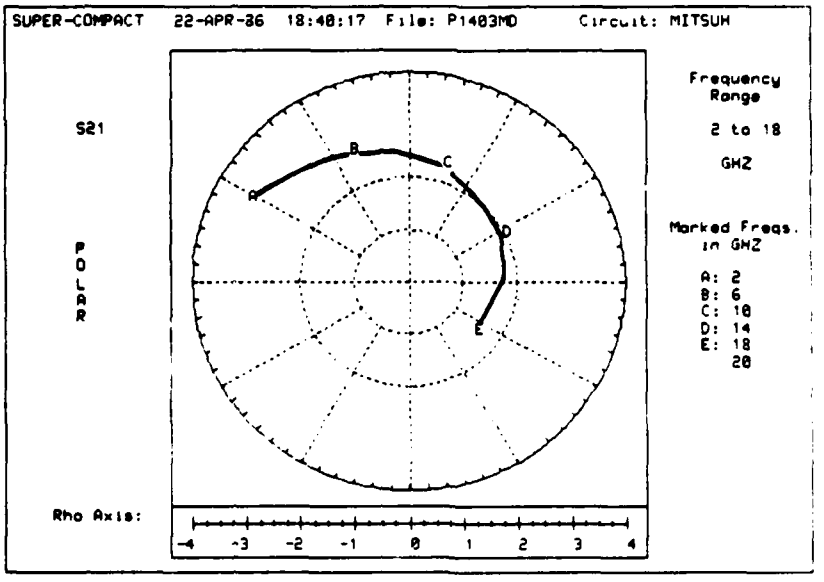


Figure 23a. Mitsubishi Data Sheet 1403 S_{11}, S_{22}, and S_{21}. Ids = 30 mA

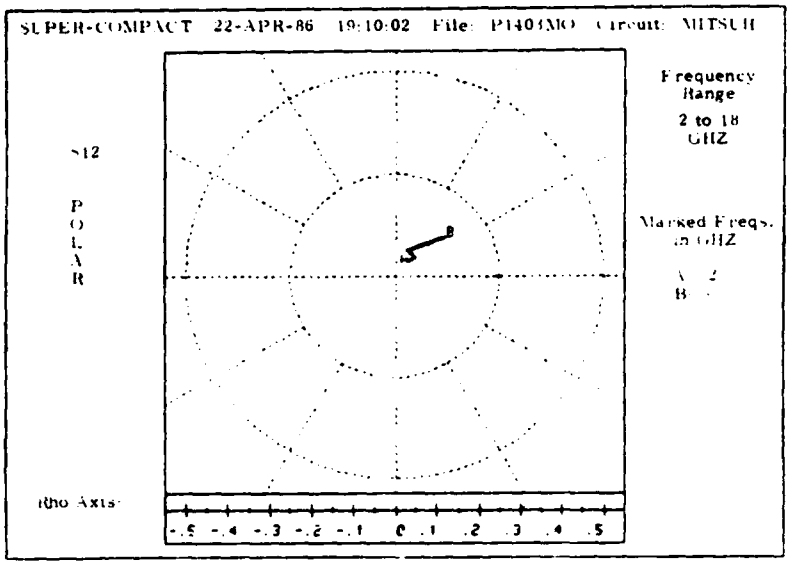


Figure 23b. Mitsubishi Data Sheet 1403 S_{12}.
Ids = 30 mA

4.2 DC Characteristics

Once the FET chips were mounted into the D-13 substrate and electrically connected to the CPW using the Westbond machine, they were tested for their DC characteristics. This was done to determine if they had been damaged during the mounting or bonding process. At any point, the chip could easily be destroyed by careless handling or from the discharge of static electricity. Although bad DC characteristics would indicate a bad chip and guarantee unacceptable RF performance, it is possible for the FET to display good DC characteristics and yet still behave poortly at RF. This happened at least twice. Figure 24 shows typical measured DC characteristics of 1403 and 1404 FET chips mounted in K-connector fixtures. According to the data sheet, there is a rather large window of acceptable values for the saturated drain-to-source current (Idss). From Figure 24, it appears that the FET chips used in this project fall within the acceptable range.

4.3 FET-in-Hole Mounting Technique

Initially the 10 GHz amplifier was to be built using the SMA test fixtures containing tapered CPW lines. The center section of the taper was made narrow to allow very short bonds between the source terminals of the FET and the ground planes of the CPW. Two SMA test fixtures were built containing 1403 GaAs FET chips. Each chip was mounted into a tapered CPW line that was etched on gold-metallized D-13. The D-13 substrate was 0.063-in. thick. The FET chip was mounted in a hole drilled in the center of the narrow section of the CPW taper.

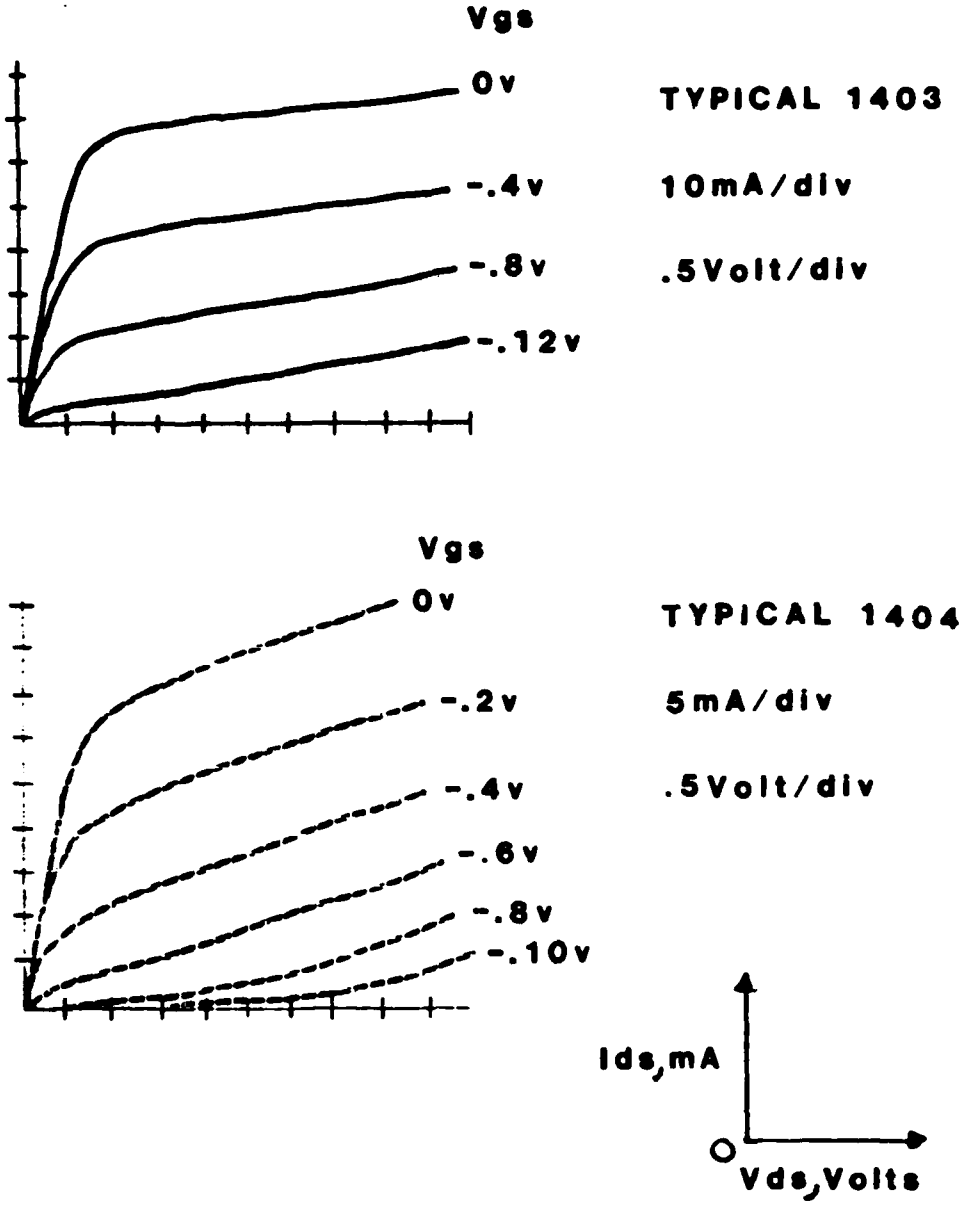


Figure 24. Typical Measured DC Characteristics of FET Chips Mounted in K-connector Test Fixtures

K-12 epoxy (ER = 12) was used to secure the FET in the hole such that the chip's surface was flush with that of the substrate. The diameter of the drill was chosen to be nearly equal to the S+2W dimension of the narrow section of the taper. The holes were drilled using a drill press onto which a microscope had been attached. Gold wires of 0.0008-in. diameter were used to attach the chip to the CPW. The attempted arrangement is depicted in Figure 25. In practice it was impossible to drill a neat, centered hole. The result was more like a crater, and excessively

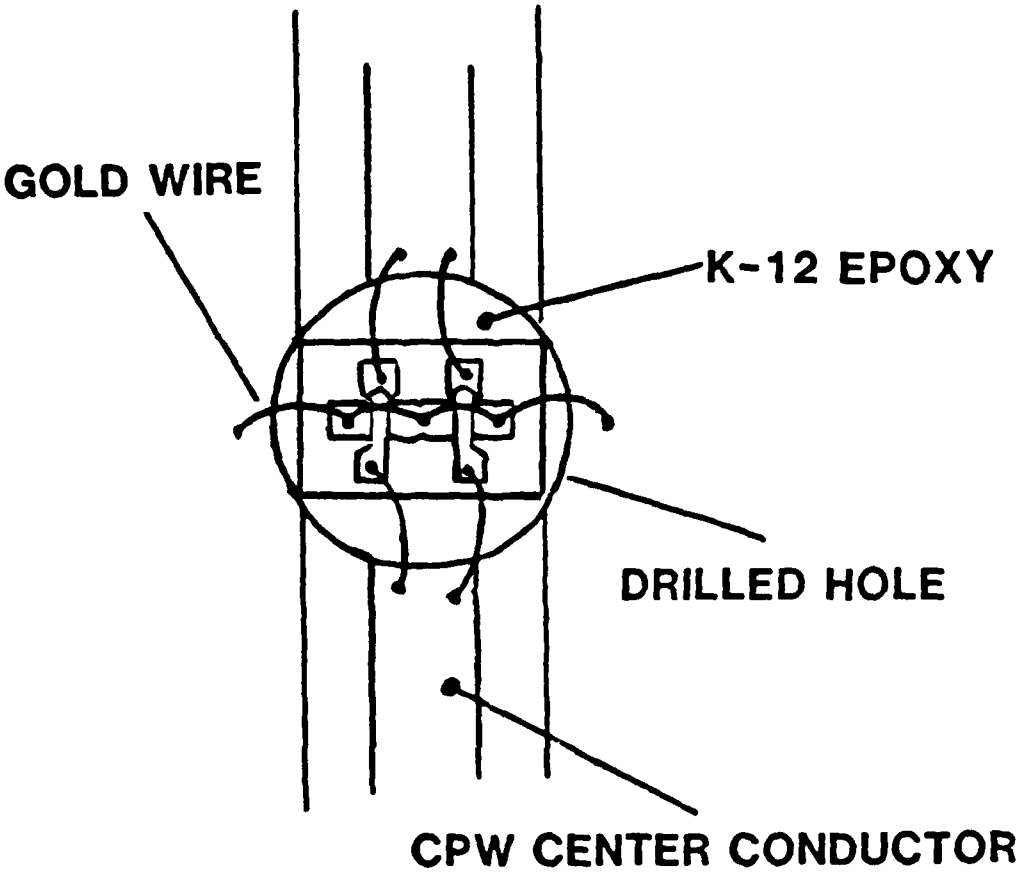


Figure 25. Initial Mounting Technique for FET Chips

long bond wires had to be used to connect the chip to the CPW, inserting an inductance in series between the chip's terminals and the rest of the circuit. Figure 26 shows the de-embedded S_{11} and S_{22} of a 1403 FET chip mounted in a hole. Note that both S_{11} and S_{22} are more inductive than the data sheet S_{11} and S_{22}. Inductance in series with the gate and drain is not a great problem for a narrowband amplifier design—it simply changes the s-parameters that must be matched to 50 Ω at the design frequency. Inductance on the source, however, decreases the maximum available gain (MAG) or maximum stable gain (MSG) of the FET chip. This decrease is straightforward to derive from a simple circuit model of the FET. Both MAG and MSG refer to the amount of gain the FET can provide in an optimum amplifier design. The MSG is used in place of the MAG when the FET chip is potentially unstable. The length of the bond wires for a 1403 mounted in a hole was measured and their inductance calculated from a formula from Ha.[3] Figure 27 is a plot of

the MAG or MSG (whichever is appropriate) calculated from the de-embedded 1403 s-parameters, the s-parameters from the Mitsubishi data sheet, and the data sheet s-parameters with the excess source inductance calculated above included. Note the effect of the excess source inductance. Because of the long source wires, this mounting scheme was abandoned. A new method was devised, and all further de-embedding was done using 0.025-in. thick substrates and the K-connector fixtures.

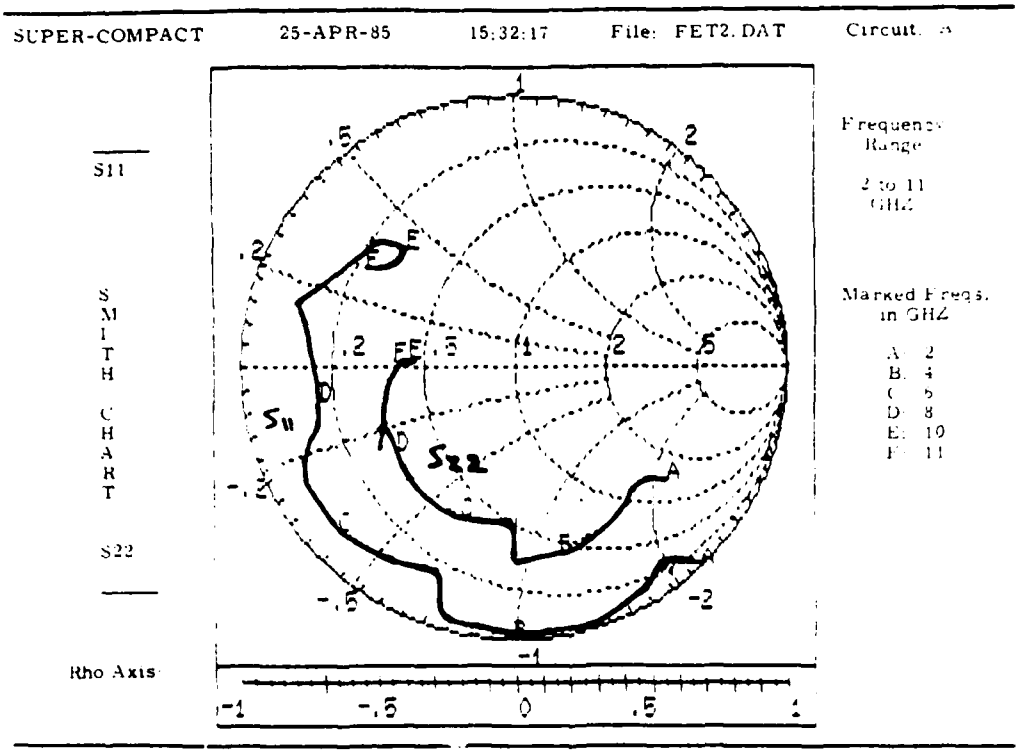


Figure 26. De-embedded S_{11} and S_{22} of 1403 GaAs FET Chip Mounted Into a Drilled Hole

4.4 FET-in-Groove Mounting Technique

Figure 2 shows the second mounting technique tried. A groove of the exact width of the FET (0.015 in.) and approximately 0.010-in. deep was cut into the substrate, in a direction perpendicular to the CPW transmission line. K-12 epoxy was used to secure the FET and to fill in the rest of the groove. Gold ribbons were cut, under a microscope, to lengths of approximately 0.018 in., and small tabs for contacting the source pads of the FET were cut into the sides. The tabs were approximately 0.003-in. wide by 0.005-in. long. The ribbons were bonded across the groove and the tabs bonded to the FET chip, as indicated in Figure 2. Gold wires of 0.0008 in. diameter were used to connect the gate and drain terminals to

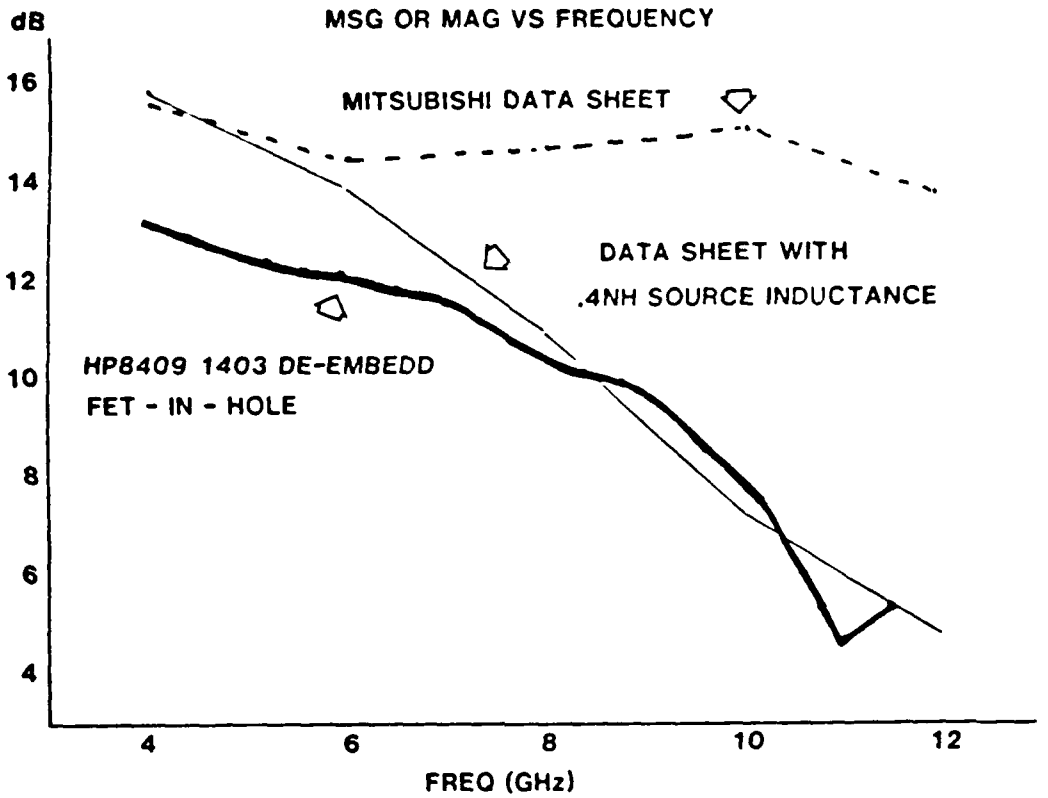


Figure 27. MSG or MAG of 1403 GaAs FET Chips

the CPW center conductors. The groove was cut by outside vendors using a DISCO substrate dicing machine and a 0.015-in. wide dicing saw. Through the use of a television camera and a microprocessor, an operator of this machine can very accurately control the location and depth of a cut. The CPW lines were etched onto the gold-metallized D-13 prior to the grooving operation. A 0.015-in. slot was etched also, exactly where the groove should be placed, to aid in positioning the saw. All the 50-Ω CPW lines used a S of 0.010 in. and W of 0.007 in., for an S+ 2W dimension of 0.024 inch. To test the mounting arrangement, a substrate was prepared as indicated above, but instead of installing a FET chip in the groove, a 0.010-in. wide ribbon was bonded across the CPW center conductors. Gold ribbons without tabs were used to connect the ground planes. The measured s-parameters of the test circuit were very similar to those of a straight 50-Ω line etched on an ungrooved substrate, indicating that the mounting technique is electrically sound. This mounting technique allowed much more precise placement of the FET chip than the previous, FET-in-hole method. It was used for both the 10 GHz and 20 GHz amplifiers.

4.5 10 GHz S-parameters

As previously discussed, the data used to de-embed the s-parameters used to design the 10 GHz amplifier was measured on an HP 8409 network analyzer employing an eight-term error model. Three K-connector fixtures containing through lengths of 50-Ω line were built—the transmission line lengths were 0.500 in., 0.550 in., and 0.600 inch. Prior to de-embedding a GaAs FET chip, a 50-Ω line was de-embedded to determine if any gross errors existed in the computer programs or in the method. The two shortest fixtures were used as THRUS and THRUL in DMBED.FOR to obtain the error terms of the embedding network, which in this case consisted of a K-connector, a transition to the CPW, and a 0.250-in. length of CPW transmission line. The calculated error terms were then used to de-embed the fixture with the 0.600-in. length of transmission line, yielding the s-parameters of a 0.100-in. length of 50-Ω CPW line. There was obviously at least 0.35 dB error in the magnitude of S_{21}, as the magnitude of the de-embedded transmission coefficient of the 0.100-in. length of CPW was a positive 0.35 dB at 3 GHz. The return loss of the 0.100-in. section was around 20 dB up to the maximum measurement frequency of 12 GHz. The phase of S_{21} was within a few degrees of the calculated value of 90°.

A total of three 1403 FET chips, labeled FETX, FETY, and FETZ, were de-embedded using the fixtures containing the 0.500-in. long and 0.600-in. long transmission lines as THRUS and THRUL. The $\Delta\ell$ of 0.100 in. was deliberately chosen to be close to 90° in electrical length at 10 GHz, to minimize the susceptibility to error of the de-embedding equations. A quick look at the de-embedding equations will verify that this is the best choice, considering the sine term in the denominators. The FET chips were de-embedded at both the low (Ids = 10 mA) and high (Ids = 30 mA) bias current levels. FETY was accidently reverse biased and was damaged. The MAG or MSG calculated from both the low noise and high gain s-parameters is plotted in Figure 28. The 10 GHz MAG or MSG is higher than the FET-in-hole case, but it is still not as high as that calculated from the data sheet s-parameters.

Conversations with a representative from Mitsubishi and another engineer,[11] who has authored a paper on de-embedding, revealed that it is not uncommon to obtain less MAG or MSG than a manufacturer claims for its device. One potential reason for this is simple—FET chips vary from lot to lot. Another possibility is that of signal transmission around the FET changing the s-parameters measured and altering the MAG or MSG. The S_{12} of the FET chip is very small and any path

11. Telephone conversations with Thomas Costa, a sales engineer with Mitsubishi, and John Eisenburg, author of an article on the TSD de-embedding technique, which appeared in Microwaves and RF, November 1985.

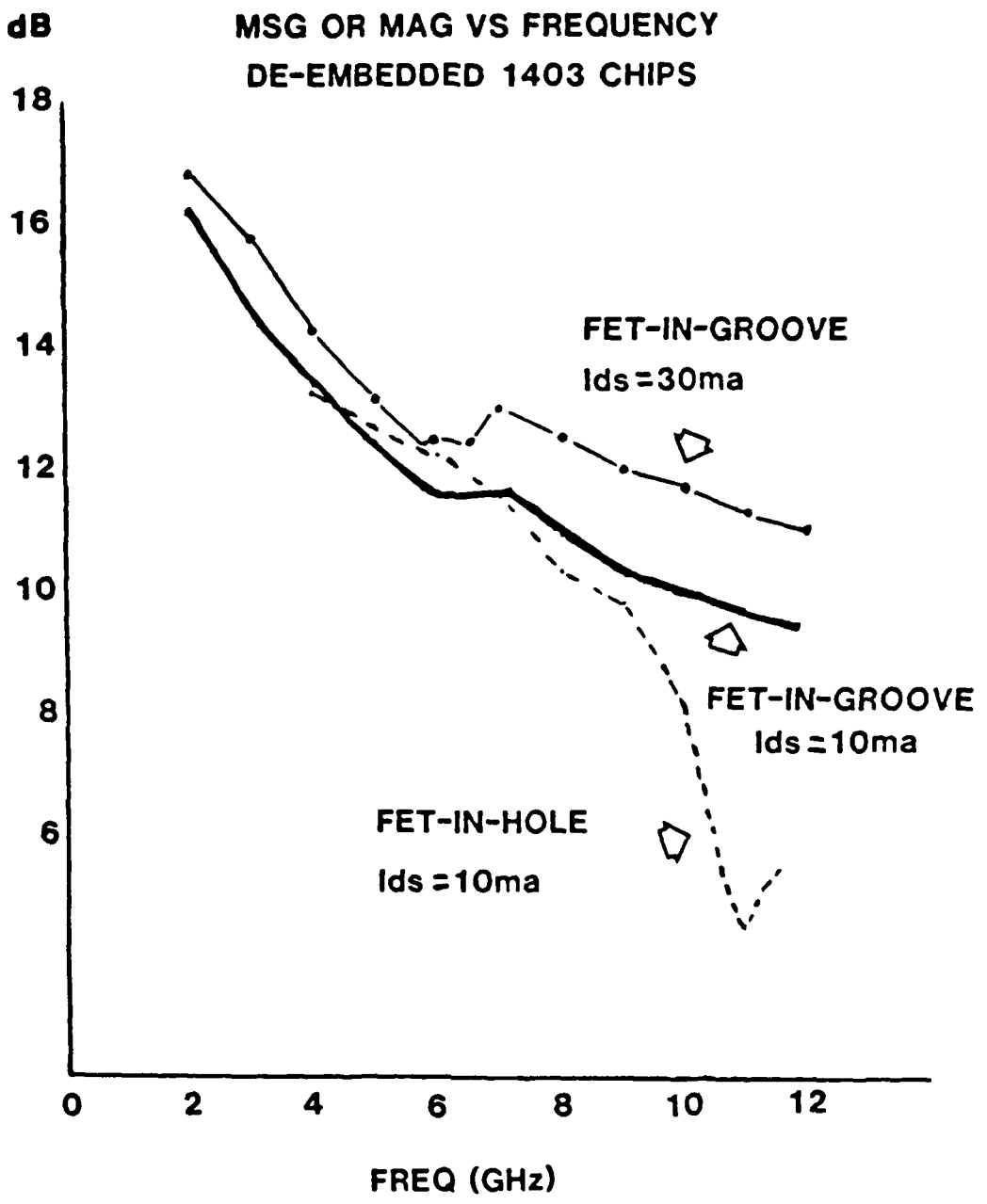


Figure 28. MSG or MAG Calculated From De-embedded s-parameters of 1403 GaAs FET Chips for Two Different Methods of Mounting the Chip

in parallel with the FET could considerably change the value of this parameter that is measured for a device mounted in a circuit. The effect of a signal path in parallel with the FET chip can be checked by de-embedding the s-parameters of a mounted but unbonded FET as well as the s-parameters of a bonded, biased FET chip. Both s-parameters are converted to y-parameters, and the y-parameters for the unbonded FET are substracted from the y-parameters for the bonded, biased

FET chip. The result is converted back to s-parameters and used to calculate the MAG or MSG. This was not done. Although it would have been informative, it would not have solved any problems – the FET chip would still have to be used as mounted, and the MAG originally calculated would be valid.

The 10 GHz amplifiers were designed using an average of the de-embedded s-parameters of FETX and FETZ at a drain-to-source current of 30 mA. These s-parameters are plotted in Figures 29a and 29b. A low-noise amplifier design

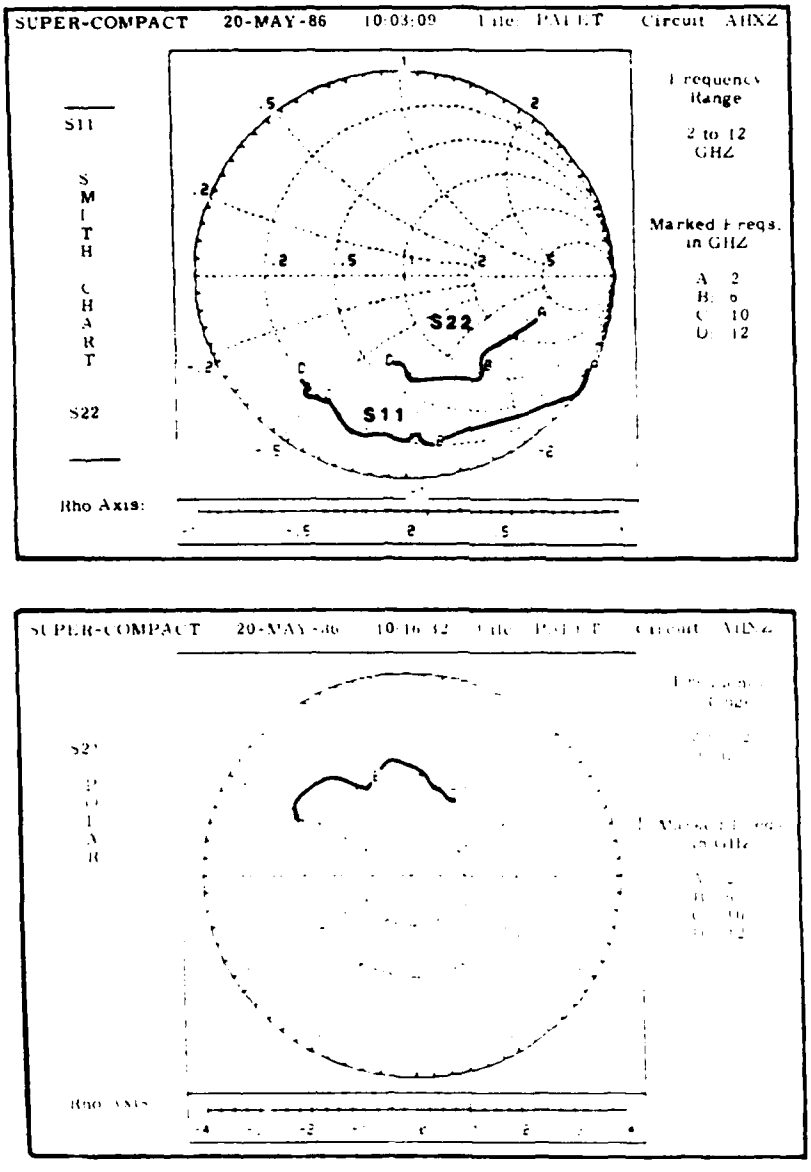


Figure 29a. De-embedded 1403 S_{11}, S_{22}, and S_{21} Used for 10 GHz Amplifier Design. Each plotted s-parameter, S_{ij}, is an average of the de-embedded s-parameters, S_{ij}, of FETX and FETZ. Data taken on an HP 8409 employing eight-term correction. Ids = 30 mA

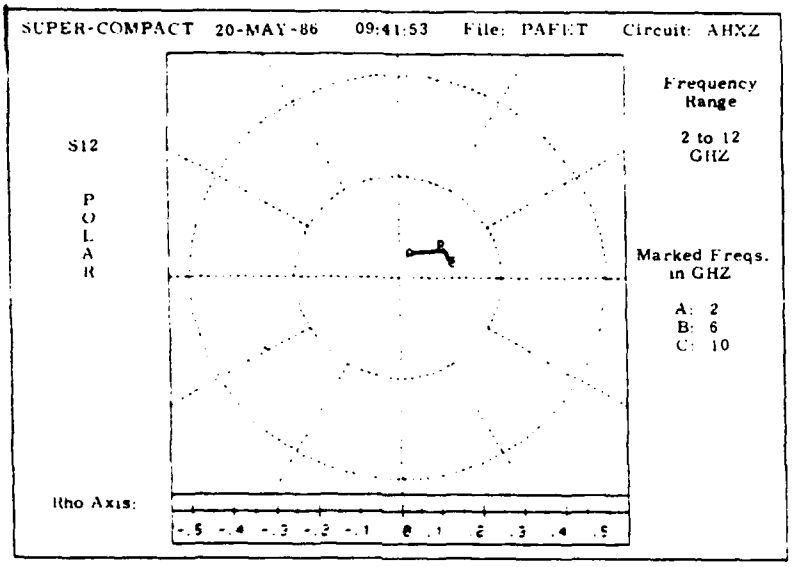


Figure 29b. De-embedded 1403 S_{12} Used for 10 GHz Amplifier Design. The plotted S_{12} is an average of the de-embedded S_{12} of FETX and FETZ. Data taken on an HP 8409 employing eight-term error correction. Ids = 30 mA

was initially considered, but because the MAG or MSG calculated from the low-noise bias condition s-parameters was not felt to be high enough, the idea was abandoned. The associated gain would most likely have been even less than the maximum available gain. It was decided to build a maximum gain small-signal amplifier instead, based on the high-gain s-parameters.

4.6 20 GHz S-parameters

The Mitsubishi 1404 FET chip was used for the 20 GHz amplifier. The 1404 has a 0.3-μ gate length and was expected to have a higher MAG or MSG at 20 GHz than the 1403, which has a 0.5-μ gate length.

All the FET chips supplied to the author by Mitsubishi were metallized with gold on the backside of the chip. The author was unsure of the effect of this ground plane on the de-embedded s-parameters, or of the degree to which it compromised efforts to mount the chip in a truly monolithic fashion. A true monolithic FET in CPW, of course, will not have a floating ground plane 0.004-in. below the surface of GaAs. To test the effect of the ground plane on chip performance, the author

removed the ground plane from a 1403 chip by placing the chip upside down on a thin film of photoresist on a glass side and immersing the slide in gold etchant. Unfortunately, the de-embedded s-parameters of this 1403 chip were very strange, indicating that it more than likely had been damaged during handling, and that any comparison between the ungrounded 1403 and the other 1403 chips could be inconclusive. However, the author improved his laboratory technique and successfully removed the ground planes from all the 1404 chips used in this project, to better model a monolithic environment and to eliminate any effect the ground plane could have on the chip's performance.

Data for the de-embedding of the 1404 chips was taken on a HP 8510 network analyzer, rather than on the HP 8409 used for the de-embedding of the 1403 s-parameters. Again, a 50-Ω line was de-embedded first to test the procedure. The de-embedded return and insertion loss of the approximately 0.500-in. long CPW line are shown in Figures 30a and 30b. The return loss is better than that obtained when de-embedding a 50-Ω line using data taken using the HP 8409 network analyzer.

Two different methods were used to measure the test fixtures on the HP-8510 network analyzer. In one method, the fixtures were made insertable by placing APC-7 to APC-3.5 adapters on each end of the test fixtures. The second method involved the "switched-adapter" technique. The measurements and these techniques were elaborated on in Section 3. Both methods yielded similar results. To help eliminate any errors in the de-embedded s-parameters arising from electrical discrepancies between any of the test fixtures, three test fixtures were used to obtain two sets of error terms representing the embedding networks. The 1404 FET chip's s-parameters were de-embedded using each set and were then averaged. Using TRANS2 (L = 0.500 in.) as THRUS and TRANS3 (L = 0.550 in.) as THRUL, one set of error terms was calculated, and then, using TRANS3 as THRUS and TRANS4 (L = 0.600 in.) as THRUL, a second set was calculated. In both cases, $\Delta\ell$ = 0.050 in., corresponding to an electrical length near 90° at 20 GHz. TRANS2 and TRANS4 could not be used to determine the 20 GHz error terms, because a $\Delta\ell$ of 0.100 in. corresponds to an electrical length near 180° at 20 GHz. The 1404 chips were de-embedded at Ids levels of 10 mA and 30 mA, and the 30 mA current level was used for the design of the 20 GHz amplifiers.

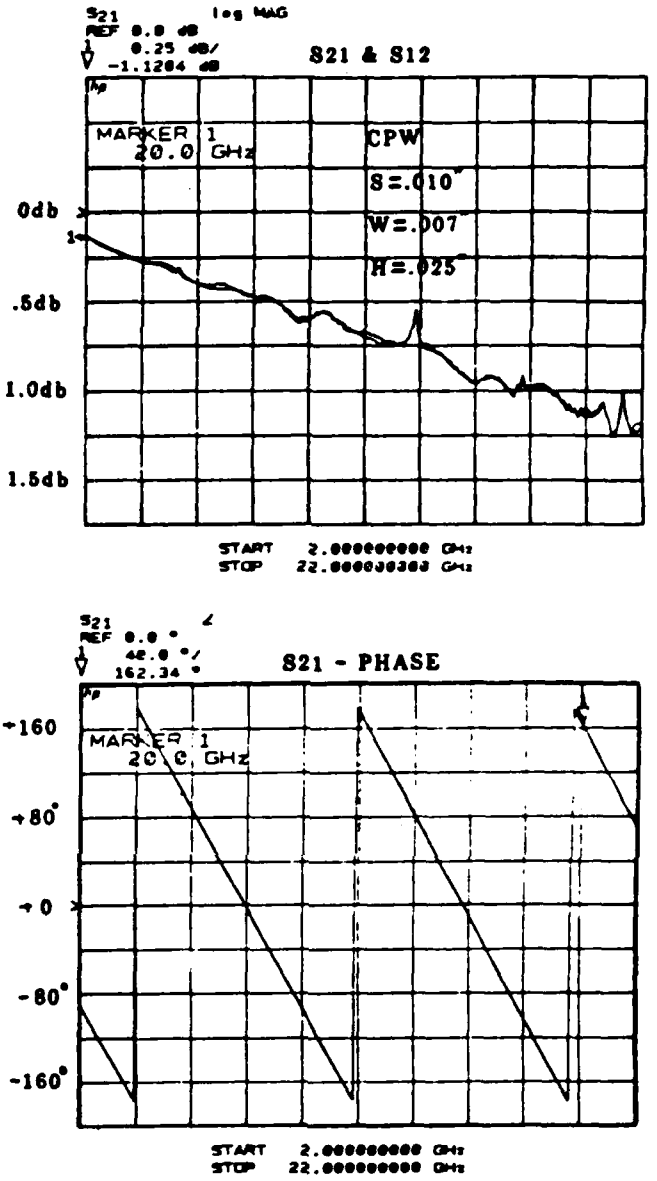


Figure 30a. De-embedded Insertion Loss of a 50-Ω CPW Line of an Approximate Length of 0.500 inch. (S = 0.010in., W = 0.007 in., H = 0.025 in.)

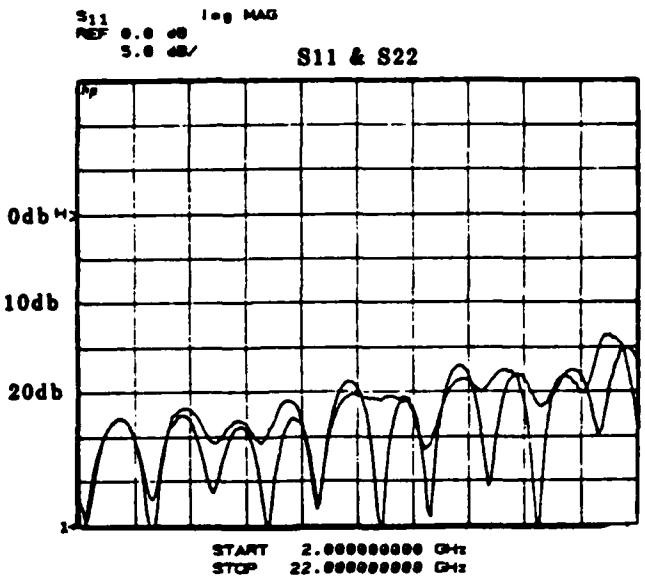


Figure 30b. De-embedded Return Loss of a 50-Ω CPW Line of an Approximate Length of 0.500 inch. (S = 0.010 in., W = 0.007 in., H = 0.025 in.)

Two separate efforts were made to de-embed the s-parameters of 1404 chips. The first effort provided the s-parameters used for the 20 GHz design, but because the 20 GHz amplifiers behaved poorly, a second effort was required to determine if the design had been based on erroneous s-parameters. In the second de-embedding attempt, two 1404 FET chips were de-embedded and both were found to have very similar s-parameters, but these s-parameters were very different from those obtained in the first effort. Figures 31a and 31b show a comparison between the s-parameters obtained in the first and second de-embedding efforts. The "BUILD" s-parameters are those of the second effort and the "DESIGN" s-parameters are those of the first effort. Figure 32 is a plot of the MSG or MAG calculated from both the "BUILD" and "DESIGN" s-parameters. The two curves in Figure 32 are very close—both the "DESIGN" and "BUILD" s-parameters can provide the same gain.

However, the differences between the "DESIGN" and "BUILD" s-parameters are real. All the FET chips were de-embedded several times and the s-parameters plotted in Figures 31a and 31b always resulted. The K-connectors in the test fixtures containing the "DESIGN" FET chip were changed to ensure that a connector was not responsible for the "DESIGN" s-parameters. Also, there is not a reference plane error in the de-embedded "DESIGN" s-parameters. The "DESIGN" chip's S_{21} was also de-embedded using a simpler and much less accurate method.

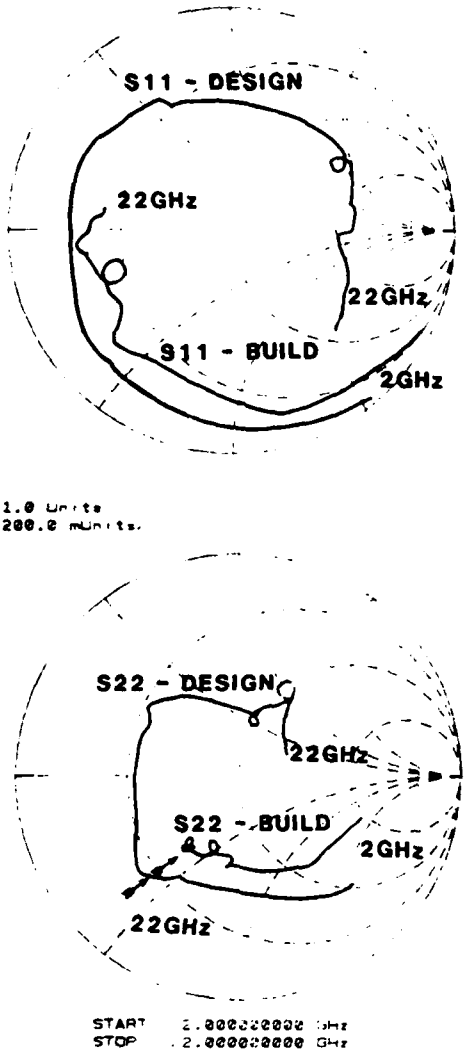


Figure 31a. De-embedded S_{11} and S_{22} of "DESIGN" and "BUILD" Mitsubishi 1404 GaAs FET Chips

A "thru" fixture the same length as the test fixture containing the "DESIGN" FET was measured on the HP 8510, and the S_{21} of this fixture used to divide the S_{21} measurement of the fixture containing the "DESIGN" FET chip. The resulting curve showed the same phase behavior as the S_{21} obtained through the use of the more accurate de-embedding method.

The author did notice that the CPW line in which the "DESIGN" FET was mounted contained a considerable amount of gold in the slots; the quality of the etching job was quite poor. The CPW line was not shorted at DC, but it is hard to predict the effect of the extra metal in the slots on the microwave characteristics

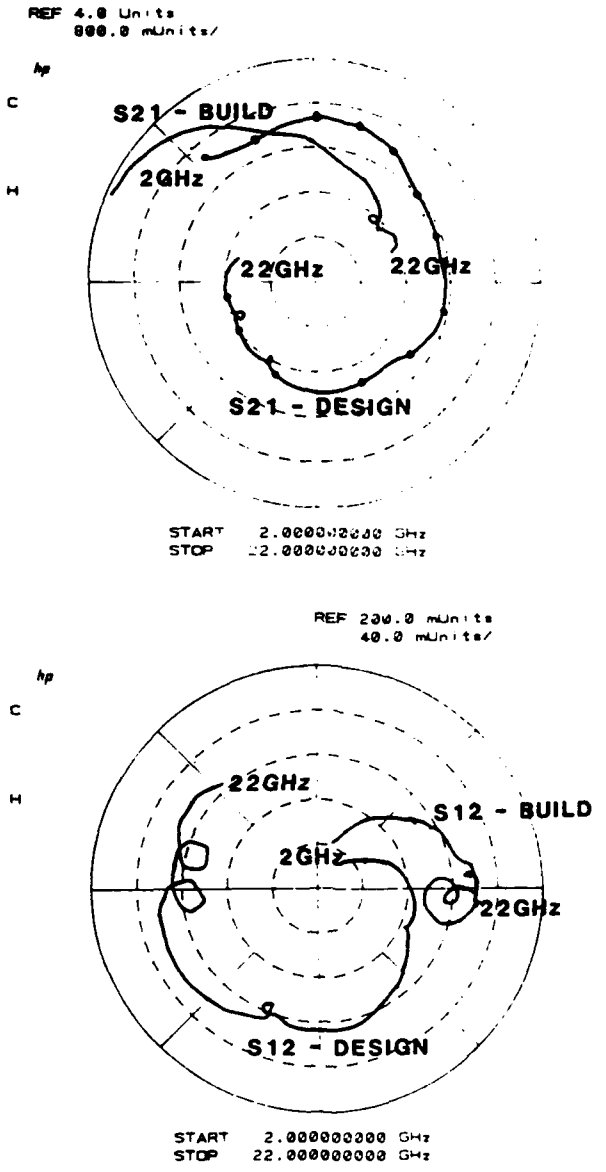


Figure 31b. De-embedded S_{12} and S_{21} of "DESIGN" and "BUILD" Mitsubishi 1404 GaAs FET Chips

of the CPW Line. Perhaps it is responsible for the extra phase shift in all the "DESIGN" FET s-parameters. It is interesting to note that metal has been included in the slots of CPW lines to build slow-wave structures. If the slots of a CPW line are periodically bridged with conducting material, the resulting structure

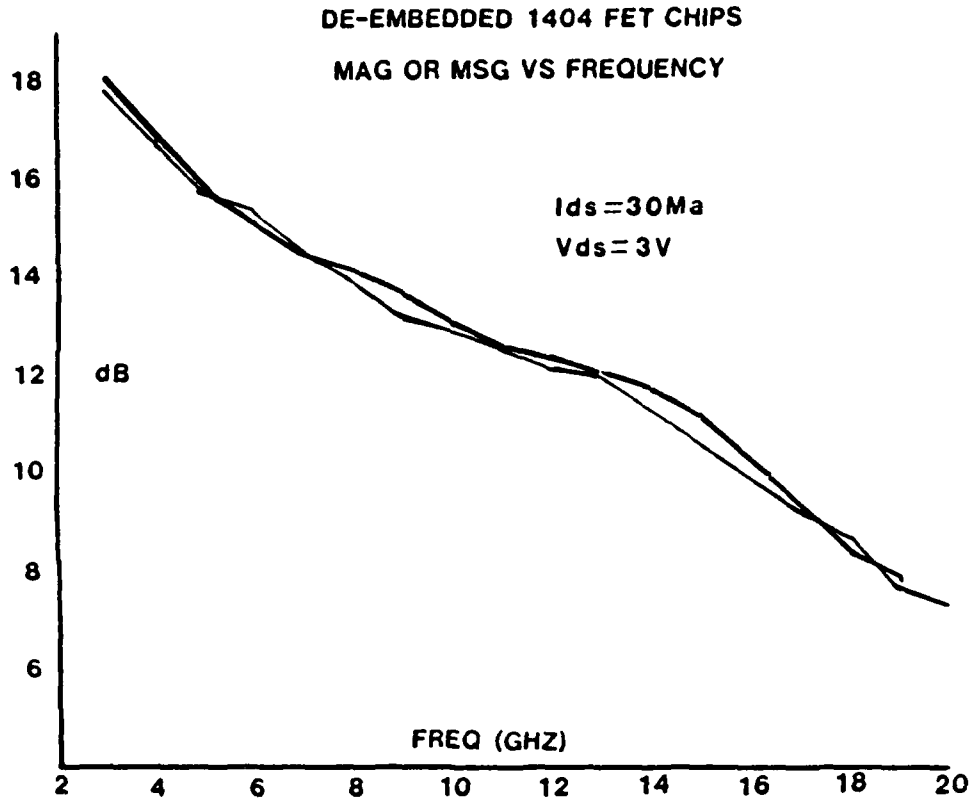


Figure 32. MAG or MSG Calculated From De-embedded s-parameters of "DESIGN" and "BUILD" 1404 GaAs FET Chips

is called Cross-Tie Coplanar Waveguide (CTCPW). CTCPW has been described in the literature as supporting slow waves.[12]

The second de-embedding effort demonstrated conclusively that the s-parameters used for the design were incorrect, and that this was the cause of the poor amplifier performance. With the "BUILD" s-parameters in a circuit model of the 20 GHz amplifier, SUPERCOMPACT® correctly predicted the actual lab performance of the 20 GHz amplifiers.

The 20 GHz design was based solely on the de-embedded s-parameters of one FET chip, and in retrospect, this was an unfortunate mistake. However, at the time an automated procedure had not been developed for transferring data from the HP 8510 to the VAX™ 11/730 computer. The author, using printouts from the HP 8510, had to type the data by hand into the computer, and it literally took hours to place all the data points from just one test fixture into a computer file. Moreover,

12. Bastida, E. M. et al (1982) Slow-wave and coplanar monolithic GaAs circuits, European Microwave Conference 1982 Proceedings, Helsinki, Finland, pp. 256-261.

the data was being taken at the University of Massachusetts in Amherst and analyzed on the computer at RADC at Hanscom AFB. As usual, the de-embedding at first did not work because of measurement or other error, and all the necessary data had to be retaken and retyped. Two chips were to be de-embedded in this initial effort, but, after successfully building 15 or so test fixtures, the author finally built an electrically bad test fixture, and so only one chip, the "DESIGN" chip, was de-embedded. Due to limited number of 1404 chips the author had in his possession, the rest of the 1404 chips had to be saved for the construction of the amplifiers, especially since the yield in this step was not expected to be 100 percent.

4.7 CPW Loss

Two experimental methods were used to determine the attenuation in the 50-Ω CPW line used in this project, and the two methods gave nearly the same result. In method 1, TRANS2 (L = 0.500 in.) and TRANS3 (L = 0.550 in.) were used as THRUS and THRUL to de-embed a nearly 1-in. long piece of 50-Ω line mounted in a K-connector test fixture. The result of this method was the s-parameters of a nearly 0.500-in. long piece of 50-Ω line, and the de-embedded S_{21} of this line, divided by its length, was taken to be equal to the attenuation constant for travelling waves of the line. In method 2, the S_{21} of TRANS3 (L = 0.550 in.) and the S_{21} of TRANS4 (L = 0.600 in.) were each plotted, a line drawn through each curve to average out the effects of mismatch loss, the two lines subtracted, and the result divided by the difference in length of the two fixtures. As indicated in Figure 33, the attenuation predicted by SUPERCOMPACT® does not agree very well with that experimentally determined. The variables in the SUPERCOMPACT® analysis include, in addition to the dimensions of the CPW line and the thickness and relative dielectric constant of the substrate, the loss tangent and the surface roughness of the substrate. TRANS-TECH, the manufacturer of the D-13 substrate material, claims a loss tangent of 0.0001 at 10 GHz and an rms surface roughness of less than 10 micro-inches.

There are several potential reasons why the measured loss data do not agree with that calculated by SUPERCOMPACT®. The loss tangent and/or the surface roughness claimed by TRANS-TECH may be wrong. Also, the quality of the etching job may have been poor, as in the case of the 1404 de-embedding effort. The author examined many of the substrates under a high-power microscope and found the surfaces of the substrates to contain many inclusions. The inclusions in the CPW slots often contained unetched metal. It is impossible to predict to what extent this would affect the loss in the CPW, but it is probable that it does do something. For a valid

comparison between theory and experiment of the loss in CPW, a good, reliable substrate material, such as alumina, should be used to support the CPW.

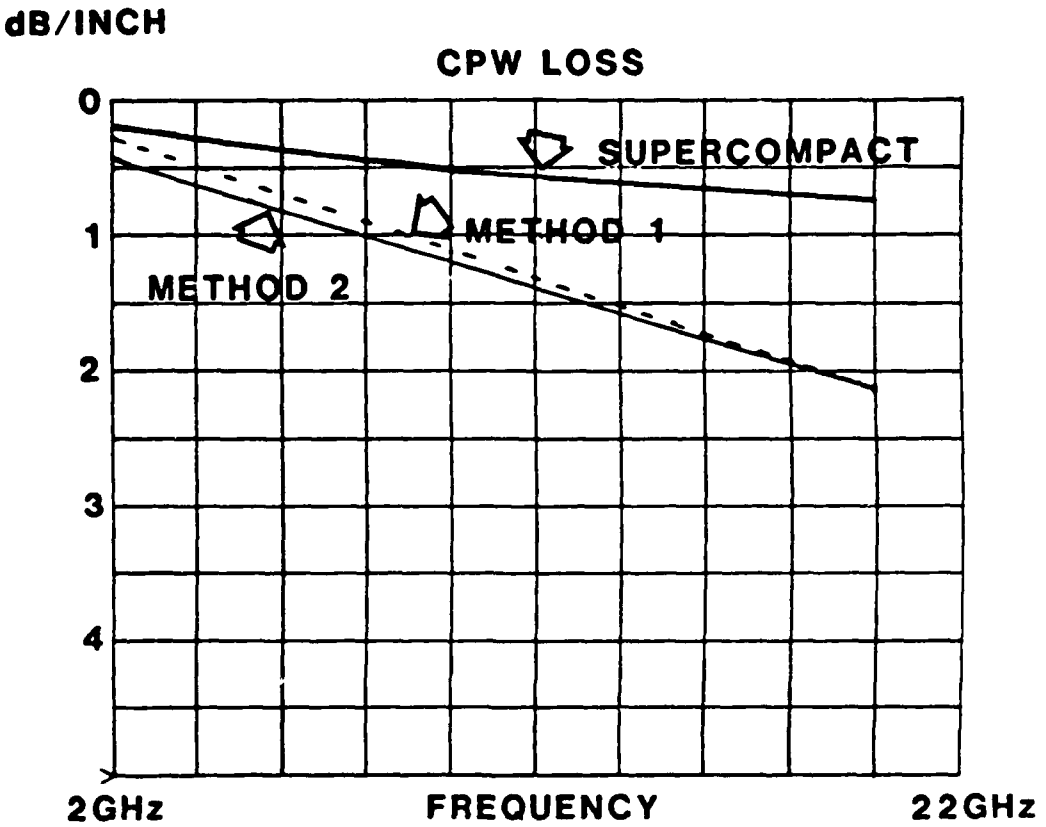


Figure 33. Measured and Predicted Loss of a 50-Ω CPW Transmission Line (W = 0.010 in., S = 0.007 in., H = 0.025 in.) Etched on Gold-metallized TRANS-TECH D-13 Substrate Material. (Er = 12.8, H = 0.025 in., loss tangent = 0.0001 at 10 GHz, rms surface roughness = 10 micro-inch)

5. DESIGN AND PERFORMANCE OF AMPLIFIERS

5.1 General Design Considerations

Figure 34 shows a simple schematic of a single-stage narrowband amplifier. The first step in designing the amplifier in Figure 34 is to find the proper values of Γ_S and Γ_L to present to the active device so that it behaves as desired at the design frequency. In this project, the design goal was to obtain the highest possible small-signal gain, and the proper values of Γ_S and Γ_L were those that maximized the transducer gain (Power delivered to load/Power available from the source) at either

10 GHz or 20 GHz. Once the Γ_L and Γ_S required at the design frequency have been determined, the next task is to design practical input and output matching networks that transform the 50-Ω source or load impedances to the necessary Γ_L or Γ_S. If the active device is potentially unstable, the Γ_S and Γ_L presented to the device by the matching circuits at all frequencies for which the potential instability exists have to be examined also. Certain values of Γ_S and Γ_L must be avoided to eliminate any possibility of oscillations. If necessary, the matching circuits are changed and the stability analysis performed again.

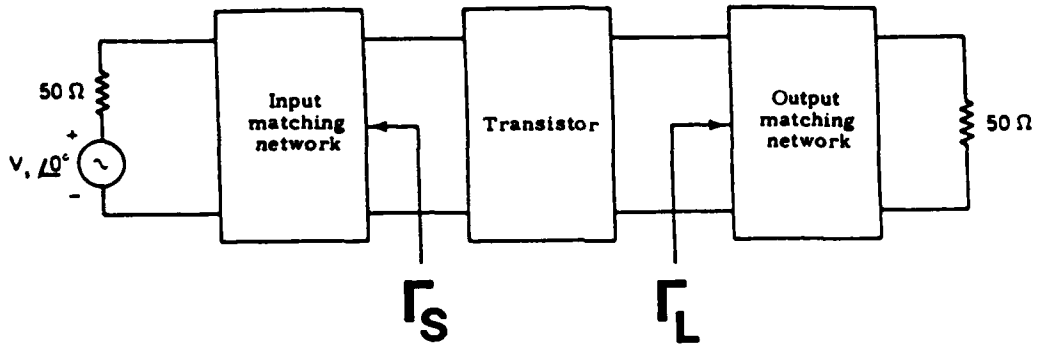


Figure 34. Simple Schematic of Single-stage Transistor Amplifier, From Gonzalez[2]

The matching networks are usually assumed to be lossless. After the design is complete, an estimate of the loss can be included in the analysis and the design altered if the performance is unacceptable. In this project, the exact loss in the matching elements was not known. Analysis on SUPERCOMPACT® revealed that any reasonable loss in the transmission lines of the matching elements simply lowered the gain of the amplifier slightly. The frequency response was not greatly affected.

Of course, the design of a power amplifier, low noise amplifier, or a multistage amplifier will involve a more complicated design procedure than just outlined. However, the two basic steps, finding the proper Γ_S and Γ_L to present to each active device, and realizing practical matching networks to produce the necessary values of Γ_S and Γ_L, are part of the design of most amplifiers.

5.2 S-Parameter Equations

Several equations based on the s-parameters of the active device must be used during the design process. Most of the equations are programmed into SUPERCOMPACT®, and the graphics capabilities of SUPERCOMPACT® were very

helpful in evaluating the various solutions of the equations and finding the best design compromises. The equations are discussed in detail and are derived in the references, and no attempt will be made to re-derive them here. However, the relevance of each of the equations to the overall design procedure is briefly discussed in this section. For a more comprehensive analysis, there are many texts that can be consulted.[2,3,4] The stability equations are a convenient starting point for a discussion of the s-parameter equations.

5.2.1 STABILITY

The reflection coefficient seen at one-port of a two-port network is a function of the s-parameters of the two-port and the reflection coefficient of the load that terminates the opposite port. If either port of the two-port has a reflection coefficient with a magnitude greater than one, the input impedance at that port has a negative real part, the two-port is capable of supplying energy to a passive termination, and the two-port could oscillate. A two-port is said to be unconditionally stable (that is, oscillations are not possible) at a given frequency if the real part of the impedance looking into either port is greater than zero for all possible passive source and load terminations. Unless the two-port network is unconditionally stable at a given frequency, it could possibly oscillate at that frequency.

The necessary and sufficient conditions for unconditional stability have been derived and can be written in several forms. The form used in SUPERCOMPACT[5] involves two factors:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 - |\Delta S|^2}{2\,|S_{12}S_{21}|} \qquad (15)$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta S|^2$$

where

$$\Delta S = S_{11}S_{22} - S_{12}S_{21}$$

If the s-parameters of the two-port satisfy $K > 1$ and $B_1 > 0$, the two-port is unconditionally stable. It is extremely important that the potential for oscillation be examined carefully at all frequencies. An amplifier designer who works only with the s-parameters of the active device for the frequency range over which he needs amplification may inadvertently design an excellent oscillator at some other frequency.

If a two-port is not unconditionally stable, it is said to be conditionally stable. There are methods of making conditionally stable networks unconditionally stable and these methods usually involve including feedback in the design or adding lossy elements near the two-port. However, it is not necessary to create an unconditionally stable two-port to be sure that oscillations will not occur. The stability circles are helpful in further specifying the condition under which a two-port can and cannot oscillate.

5.2.2 STABILITY CIRCLES

If a two-port is conditionally stable, presenting certain reflection coefficients to one port of the two-port will cause an input impedance with a negative real part to be seen looking into the other port. For example, there may be particular values of Γ_L (attached to Port 2) that cause an impedance with a negative real part at port 1. However, these values of Γ_L do not occur randomly on the Smith chart, but are confined to a definite region of the chart. Any Γ_L that causes a $|\Gamma_{in}| > 1$ is said to be in the unstable region of the output plane, and any Γ_L for which $|\Gamma_{in}| < 1$ is said to originate from the stable region of the output plane. Similarly, any Γ_S that causes $|\Gamma_{out}| > 1$ is said to be in the unstable region of the input plane, and any Γ_S for which $|\Gamma_{out}| < 1$ is said to be in stable region of the input plane.

The boundary between the stable and unstable regions of the output or the input plane is a circle, and is called the stability circle. The radius and center of the input plane stability circle and the output plane stability circle are both calculated from the s-parameters of the two-port. Either the inside of a stability circle will be the stable region and the outside of the unstable region, or vice-versa. A stability circle may be totally contained within the Smith chart, partially on the chart, or completely off it. The input plane stability circle is usually different from the output plane stability circle, and both are a function of frequency because the s-parameters change with frequency. The stability circles are significant because the device can only oscillate if either Γ_S is in the unstable region of the input plane stability circle or if Γ_L is in the unstable region of the output plane stability circle. A K-factor greater than one and positive B1 indicate that the input and output stability circles are off the chart, that the unstable region is contained inside the circles, and that the device is unconditionally stable. If the stability circles have unstable regions on the Smith chart, the device is only conditionally stable.

Although a device may only be conditionally stable, if an amplifier designer is careful to ensure that the Γ_S and Γ_L presented to the device by the matching circuits stay out of the unstable regions of the appropriate stability circles, the device will not oscillate. Stability circles are used primarily to inform the designer of the regions of the Smith chart that must be avoided. A Γ_S or Γ_L that resides in the

unstable region of its stability circle at a particular frequency does not guarantee that oscillations will occur at that frequency, but indicates that they are possible. The equations for the radii and centers of the input and output stability circles are:

Input Plane	Output Plane	
$r_S = \left\| \frac{S_{12}S_{21}}{\|S_{11}\|^2 - \|\Delta S\|^2} \right\|$	$r_L = \left\| \frac{S_{12}S_{21}}{\|S_{22}\|^2 - \|\Delta S\|^2} \right\|$	(16)
$c_S = \frac{(S_{11} - \Delta S \cdot S_{22}^*)^*}{\|S_{11}\|^2 - \|\Delta S\|^2}$	$c_L = \frac{(S_{22} - \Delta S \cdot S_{11}^*)^*}{\|S_{22}\|^2 - \|\Delta S\|^2}$	(17)

5.2.3 TRANSDUCER GAIN

Transducer gain is defined as the power delivered to load divided by the power available from source. The formula for transducer gain is:

$$G_T = \frac{|S_{21}|^2 (1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_L\Gamma_S|^2} . \quad (18)$$

This is the gain the amplifier will deliver in a 50-Ω system when lossless matching networks are used to provide Γ_S and Γ_L at the input and output ports, respectively.

5.2.4 SIMULTANEOUS CONJUGATE MATCH

The goal of this project was to build maximum gain, small-signal amplifiers. Obviously, the matching networks should provide the Γ_S and Γ_L that yield the largest possible gain. The transducer gain will be the largest when both ports of the two-port are conjugately matched to the system impedance, in this case, 50 Ω. The Γ_S and Γ_L that provide a simultaneous conjugate match are:

$$\Gamma_{MS} = M^* \left[\frac{B_1 \pm \sqrt{B_1^2 - 4|M|^2}}{2|M|^2} \right] \quad (19)$$

$$\Gamma_{ML} = N^* \left[\frac{B_2 \pm \sqrt{B_2^2 - 4|N|^2}}{2|N|^2} \right]$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta S|^2 \qquad \Delta S = S_{11}S_{22} - S_{12}S_{21}$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta S|^2 \qquad M = S_{11} - \Delta S . S_{22}^* \qquad (20)$$

$$N = S_{22} - \Delta S . S_{11}^* .$$

5.2.5 MAXIMUM AVAILABLE GAIN

The transducer gain obtained when Γ_{MS} and Γ_{ML} are provided to the two-port is known as the Maximum Available Gain (MAG). The equation for the MAG can be written in terms of the k-factor.

$$MAG = G_{TMAX} = \frac{|S_{21}|}{|S_{12}|} (K - 1\sqrt{K^2 - 1}) . \qquad (21)$$

If the two-port is unconditionally stable, then $K > 1$, and using Γ_{MS} and Γ_{ML} will give a transducer gain given by the formula above. If the two-port is only conditionally stable, Γ_{MS} and Γ_{ML} are not used, and the maximum gain is known as the Maximum Stable Gain (MSG). The formula for the MSG is:

$$MSG = \frac{|S_{21}|}{|S_{12}|} . \qquad (22)$$

If the MSG is to be obtained, Γ_S and Γ_L must reside right on the edges of the unstable regions of their stability circles. If the active devices are made unconditionally stable through the addition of resistors or feedback to the circuit, there will not be any unstable regions on the Smith chart and the MAG of the active device and its stabilizing elements will be equal to the MSG of the unstabilized circuit.

5.2.6 GAIN CIRCLES

If a two-port is unconditionally stable, the highest possible transducer gain (without feedback) is the MAG. If a two-port is only conditionally stable, the highest possible transducer gain is the MSG. For each value of transducer gain less than the highest possible transducer gain, a gain circle can be drawn for each port. For example, if a device is potentially unstable and has a MSG of 10 dB, the 8 dB gain circle for a given port is the locus of reflection coefficients that, when presented to that port by a lossless matching network, will give a constant transducer gain of 8 dB, assuming a conjugate match is maintained at the opposite port. The locus turns out to be a circle. In general, any point on a given gain circle for one-port requires a different reflection coefficient to be presented to the opposite port for a conjugate match at that port. Gain circles cannot be simultaneously used for

both ports of device. They can be drawn for the input or the output. The input port gain circle is known as the available gain circle, and the output port gain circle is called the power gain circle. More specific definitions of available and power gain are:

$$\text{Available Gain} = \frac{\text{Power delivered to load}}{\text{Power available from source}}$$

$$\text{Power Gain} = \frac{\text{Power delivered to load}}{\text{Power delivered to two-port}}$$

The formulas for the centers and radii of the gain circles are:

Available gain:

$$\text{Center} = \frac{(S_{11} - S_{22}\cdot\Delta S^{*})}{Q} \tag{23}$$

$$\text{Radius} = \frac{\left(|S_{12}\cdot S_{21}|^2 - 2K\left|\frac{S_{12}S_{21}}{g}\right| + \frac{1}{g^2}\right)^{1/2}}{Q} \tag{24}$$

$$Q = |S_{11}|^2 - |\Delta S|^2 + 1/g \tag{25}$$

$$g = \frac{G_A}{|S_{21}|^2} \tag{26}$$

$$K = \text{as previously defined} \tag{27}$$

$$G_A = \text{Gain of available gain circle} \tag{28}$$

Power gain:

$$\text{Center} = \frac{(S_{22}^{*} - S_{11} \cdot \Delta S^{*})}{Q} \tag{29}$$

$$\text{Radius} = \frac{\left(|S_{12} \cdot S_{21}|^2 - 2K\,\frac{|S_{12} \cdot S_{21}|}{g} + \frac{1}{g^2}\right)^{1/2}}{|Q|} \tag{30}$$

$$Q = |S_{22}|^2 - |\Delta S|^2 + 1/g \tag{31}$$

$$g = Gp/|S_{21}|^2 \tag{32}$$

$$Gp = \text{gain of power gain circle} . \tag{33}$$

As a gain circle is drawn for increasingly higher values of transducer gain, its radius will shrink. If, for example, the available gain circle is drawn for a value of gain equal to the MAG of a two-port, the radius of the circle will be zero, and the center will be at Γ_{MS}. The Γ_L for a conjugate match at the output will be found to be equal to Γ_{ML}.

5.2.7 CONJUGATE MATCH LOCUS

Each port of a two-port network can have a gain circle drawn for it. Each point on the gain circle requires a different reflection coefficient to be presented to the opposite port for conjugate match. The locus of points representing all possible reflection coefficients that are required at a port for conjugate match by points on the gain circle of the opposite port, is referred to in this project as the conjugate match locus. An equation is not given for this locus. SUPERCOMPACT® does not plot the conjugate match locus directly; it was mapped out by choosing a few points on a gain circle and marking on a Smith chart the reflection coefficients necessary at the opposite port for a conjugate match.

5.2.8 MISMATCH LOSS CIRCLES

Mismatch loss circles are used in conjunction with gain circles on SUPERCOMPACT® to identify other combinations of Γ_S and Γ_L that can be used to obtain a given transducer gain. If a gain circle is being used for one-port of a two-port network, mismatch circles can be used at the other port. For example, if Γ_S is chosen on the 10 dB available gain circle, a mismatch loss circle may be drawn for Γ_L such that any Γ_L chosen on the circle will yield a transducer gain that is reduced by a constant amount (the mismatch loss) from the gain circle value. The formulas for the radius and center of mismatch loss circles are as follows:

$$ML = \text{mismatch loss in dB} \tag{34}$$

$$X = 10^{-0.1(ML)}$$

$$\text{Center} = X \cdot \frac{G_M(1-S_{11}\cdot\Gamma)(S_{22}^{*} - \Delta S^{*}\cdot\Gamma)}{Q} \tag{35}$$

$$\text{Radius} = \frac{(1-X)^{1/2}}{Q} \tag{36}$$

$$G_M = \frac{1}{(|1 - S_{11}\cdot\Gamma|^2 - |S_{22} - \Delta S\cdot\Gamma|^2)} \tag{37}$$

$$Q = 1 + |S_{22} - \Delta S\cdot\Gamma|^2 \cdot X \cdot G_M \tag{38}$$

$$\Delta S = S_{11}\cdot S_{22} - S_{12}\cdot S_{21} \tag{39}$$

If the mismatch circle is calculated for Γ_S, Γ in the above equations is set equal to Γ_L and represents a point on the power gain circle. If the mismatch circle is calculated for Γ_L, Γ in the above equations is set to equal Γ_S, and represents a point on the available gain circle. In the example above, any Γ_L chosen on its 2 dB mismatch loss circle will yield a total transducer gain of 10 - 2 = 8 dB. Additional information on mismatch loss circles can be found in the SUPERCOMPACT® user manual. Each point on a gain circle generates a different set of mismatch loss circles for the other port.

5.3 CPW Matching Circuit Design

5.3.1 GENERAL CONSIDERATIONS

A large amount of theoretical and experimental work has been done on microstrip transmission lines and the matching elements that can be fabricated using microstrip lines. A sufficient amount of study has been devoted to microstrip such that the electrical effects of bends, miters, crosses and discontinuities on microstrip transmission lines can be accounted for by mathematical routines on SUPERCOMPACT®. For example, a designer using SUPERCOMPACT® can adjust the electrical length of a parallel open stub in microstrip to compensate for the excess capacitance associated with the microstrip open. Unfortunately, there has not yet been a similar body of experimental and theoretical work completed on CPW transmission lines or CPW distributed type matching elements. Various distributed matching elements are mentioned in text books such as Gupta,[1] but

it is unclear as to the frequency range over which these elements have been successfully used before, or whether they behave well for all possible aspect ratios of the CPW line. Both series and parallel stubs, shown in Figure 35, can be realized in CPW, but there does not seem to be a lot of examples of their use at 20 GHz. Note that parallel elements must be attached to both sides of the center conductor, as in Figure 35, to avoid generating any components of the even mode. The slots of the parallel stubs break the ground planes of the center CPW line to which they are attached. Ribbon or wire must be bonded over the center conductors of the stubs to maintain the continuity of the main ground planes. The electrical model of this circuit at higher frequencies is undoubtedly more complicated than that of simple parallel stubs.

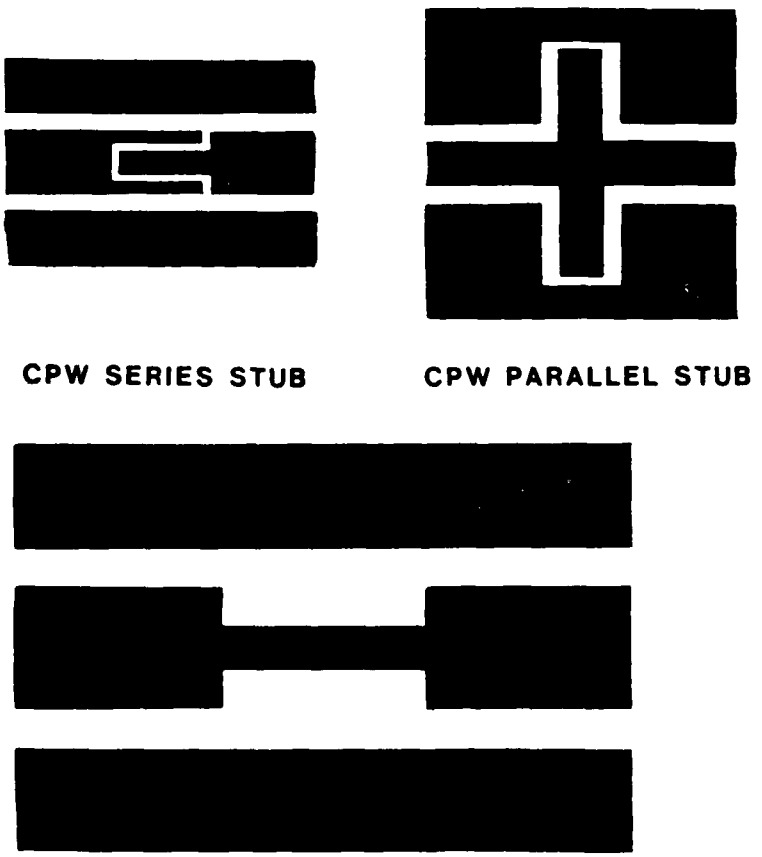


Figure 35. Some of the Matching Elements Possible in CPW

Because a matching circuit using simple elements is more likely to behave as intended than a more complicated circuit, it was decided to rely mainly on series transmission line sections for the matching elements in the amplifier designs. The discontinuities between transmission lines of different characteristic impedance levels add some uncertainty to the electrical behavior of a series transmission line matching circuit, but this is unavoidable.

5.3.2 SINGLE-SECTION MATCHING

The series transmission line section most often used for narrowband impedance matching is the quarter-wave transformer. A real load impedance of Z_L can be matched to a real impedance of Z_O by a transmission line of an electrical length of 90° whose impedance is given by: $Z_T = \sqrt{Z_O \cdot Z_L}$. If Z_L is a complex, this technique can sometimes still be used, but a little more effort is required to find the proper impedance and electrical length of the transformer section. It is helpful to use the Smith chart to visualize how a single section of transmission line can be used to match a complex Z_L to a real Z_O. As a load impedance Z_L is transformed along a Z_O-Ω transmission line, the reflection coefficient on a Smith chart normalized to Z_O Ω describes a circle with a center at 1.0 on the real axis. If a load impedance is transformed along a transmission line whose characteristic impedance is real but different from Z_O Ω, the reflection coefficient on a Z_O-Ω Smith chart still traces out a circle but the center of the circle, though on the real axis, is no longer at 1.0. Quarter-wave transformers that match real loads to Z_O Ω constitute a special family of circles. Each one of them must intersect the real axis at 1.0. The other point of intersection with the real axis is the load impedance and is related to Z_T by

$$\bar{Z}_T = \sqrt{\bar{Z}_L} \,. \tag{40}$$

The center and radius of quarter-wave transformer circles in polar coordinates on a Z_O-Ω Smith chart are given by:

$$\text{Center} = \frac{(\bar{Z}_T^2 - 1.0)}{2(\bar{Z}_T^2 + 1.0)}$$
$$\text{Radius} = |\text{Center}| \,. \tag{41}$$

Note that as the normalized transformer impedance becomes closer to 1.0, the center and radius both go to zero. Transformers with characteristic impedances less than Z_O Ω have their centers located to the left of 1.0 on the real axis, and transformers with characteristic impedances greater than Z_O Ω have

centers to the right of 1.0. Each of these circles transforms a point on the real axis to the center of the chart. However, a load impedance that happened to fall anywhere on a transformer circle can also be matched to Z_O Ω by that transformer. The problem of matching a complex load Z_L to Z_O Ω using a single series transmission line can be viewed as finding a quarter-wave transformer that matches some ficticious load Z_L' to Z_O Ω such that the transformer circle passes through Z_L. Two facts are obvious from a simple Smith chart consideration of the quarter-wave transformer circles. If the complex load Z_L resides outside the r = 1.0 or the g = 1.0 circles, the single-section series transmission line method will not work, and boundaries on the lengths of transmission line required when the method will work are determined by which quadrant Z_L is in.

Impedances outside the g = 1.0 or r = 1.0 circles can be matched to Z_O Ω if a length of transmission line of Z_O-Ω characteristic impedance is used to transform Z_L to a point inside either of the circles. Figure 36 depicts three reflection coefficients, and a series of quarter-wave circles whose normalized impedances range from 0.6 Ω to 1.5 Ω in steps of 0.1 Ω. Note that from the reflection coefficient of magnitude 0.62 cannot intersect any of the quarter-wave circles, the reflection coefficient of magnitude 0.47 just intersects the 30-Ω circle, and the reflection coefficient of magnitude 0.3 intersects several of the circles. There are several combinations of transformer impedances and lengths of Z_O-Ω line that could be used to match a reflection coefficient of magnitude 0.3 to Z_O Ω. On the other hand, it is impossible, using any length of Z_O-Ω line, to match a reflection coefficient of magnitude 0.62 to Z_O Ω using the range of transformer impedances in Figure 36. The limits on the transformer impedances that can be used to match a load of a given $|\Gamma_L|$ in a Z_0-Ω system using a matching circuit like that in Figure 37 (referred to as a single-section matching circuit) are determined by the intersection points of the circle of constant $|\Gamma_L|$ with the real axis of the Smith chart. Only values of $\bar{Z}_T$ given by:

$$Z_T \geq \sqrt{\frac{1 + |\Gamma_L|}{1 - |\Gamma_L|}} \quad \text{or} \quad Z_T \leq \sqrt{\frac{1 - |\Gamma_L|}{1 + |\Gamma_L|}} \tag{42}$$

can be used to match Γ_L to Z_O Ω. At the limit, the electrical length of the transformer section of impedance ZT1 will be 90°, and the load has essentially been rotated to the real axis and quarter-wave transformed to Z_O. The limits are plotted in the bottom half of Figure 37, for Z_O = 50 Ω. Obviously, if there is a limited range of transmission line impedances available, a single-section series matching circuit may not be appropriate.

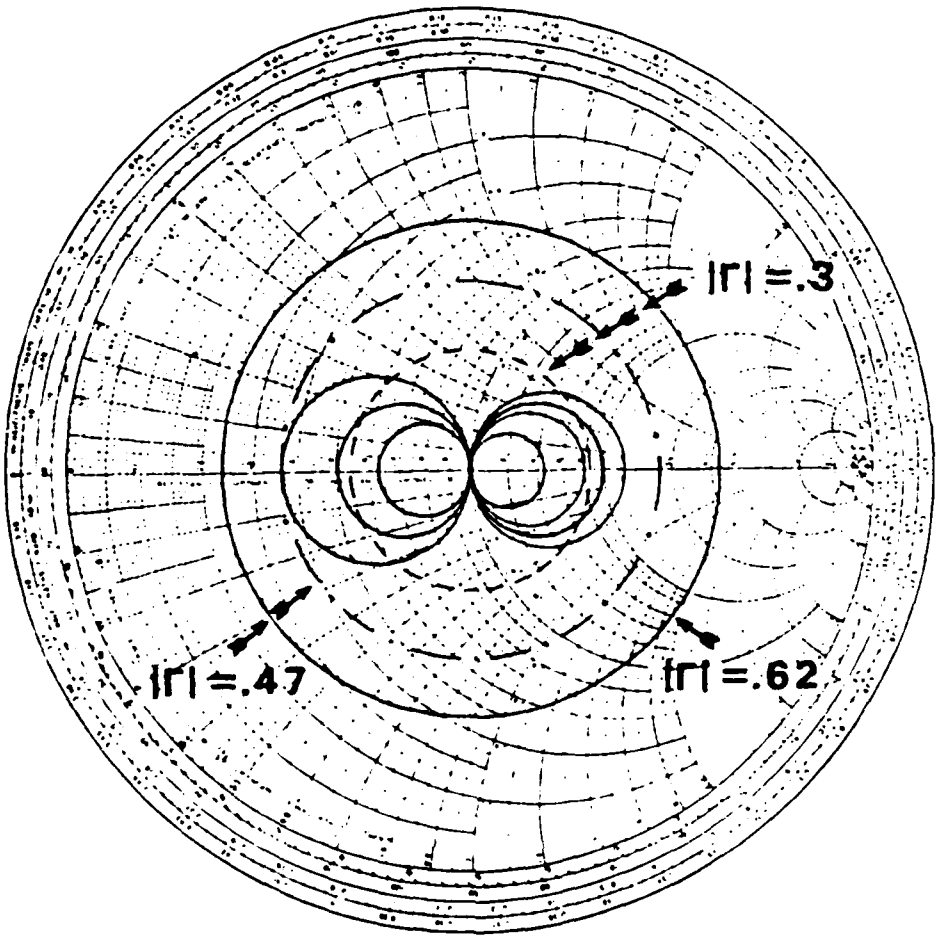


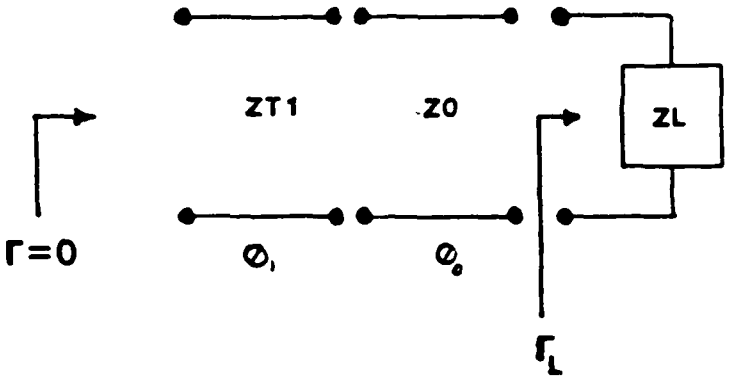
Figure 36. Smith Chart Example of Matching Complex Loads to ZO Ohms Using Two Series Transmission Lines, One of a Characteristic Impedance of ZO Ohms

A computer program was written in FORTRAN to calculate the ZT1 impedance and the electrical lengths of the Z_O and ZT1 sections that would match a complex load, Z_L, to the Z_O impedance level. The program was based on a brief article by Remillard.[13] Required as input from the user are the load reflection coefficient in the Z_O system, Γ_L, the impedance Z_O, and start, stop, and step size values for the impedance ZT1. If a match is not possible, the program prints a row of asterisks. The program is named SINGLEM.FOR.

Vendelin gives a graphical technique for finding the impedance and electrical length of the transformer section, given a load inside the r = 1.0 or g = 1.0 circle.[4] A line is drawn from the center of the Smith chart to the load impedance Z_L. The perpendicular bisector of this line is plotted and its intersection point with the real

13. Remillard, W. J. (1982) Calculator program for impedance matching, Microwave Journal, pp. 103-104.

SINGLE-SECTION MATCHING



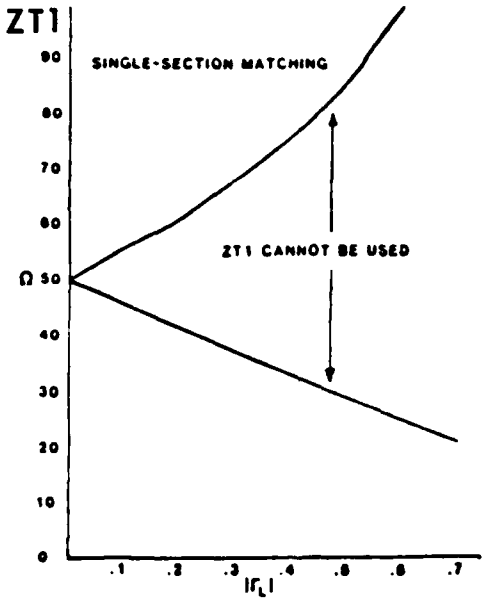


Figure 37. The Single-section Matching Technique and Limits on the Maximum Magnitude Reflection Coefficient That can be Matched to 50 Ohms Using This Technique

axis is marked. A circle is drawn whose center is at this mark and whose radius is equal to the distance between the mark and the center of the Smith chart. The square root of the intersection point of the circle and the real axis (other than the center of the chart) is equal to the normalized transformer impedance. To find the electrical length of the transformer section, the load is plotted on a Smith chart normalized to the transformer impedance. The distance in wavelengths required

to rotate the reflection coefficient in a clockwise direction to the point on the real axis representing Z_O Ω is the electrical length of the transformer section. Vendelin claims, incorrectly, that the length of the matching section will always be less than 90°.

Other techniques, requiring special graphs, have also been developed for single-section matching.[14]

5.3.3 DUAL-SECTION MATCHING

Matching a complex load impedance using two series transmission lines arranged as in Figure 38 was also investigated. In this report, the circuit in Figure 38 is referred to as a dual-section matching circuit. Two series transmission lines whose impedances are other than Z_O Ω are used, as well as a length of Z_O impedance line. For a given load reflection coefficient Γ_L, the use of a dual-section circuit allows the load to be matched using transformer impedances that can be closer to Z_O Ω than the transformer impedance required to match the load using a single transformer section. The curves on a Z_O-Ω Smith chart, representing impedance transformation along ZT1 are the quarter-wave transformer circles of the single-section technique. Contours of constant reflection coefficient on the ZT2 impedance line are offset circles of different radii and center locations. All the centers are on the real axis. The center and radius of the circle on a Z_O-Ω Smith chart representing a constant value of the magnitude of the reflection coefficient on a ZT2 impedance line are given by:

$$\text{Center} = \frac{R(\Gamma^2 - 1)}{(1 - \Gamma^2 R^2)}$$

$$\text{Radius} = \frac{\Gamma(1 - R^2)}{(1 - \Gamma^2 R^2)} \qquad (43)$$

$$R = (Z_O - ZT2) / (Z_O + ZT2) \qquad (44)$$

Γ = magnitude of load reflection coefficient on ZT2 impedance line. (45)

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14. Thomas, R. L. (1976) A Practical Guide to Impedance Matching, Artech House, Dedham, Massachusetts.

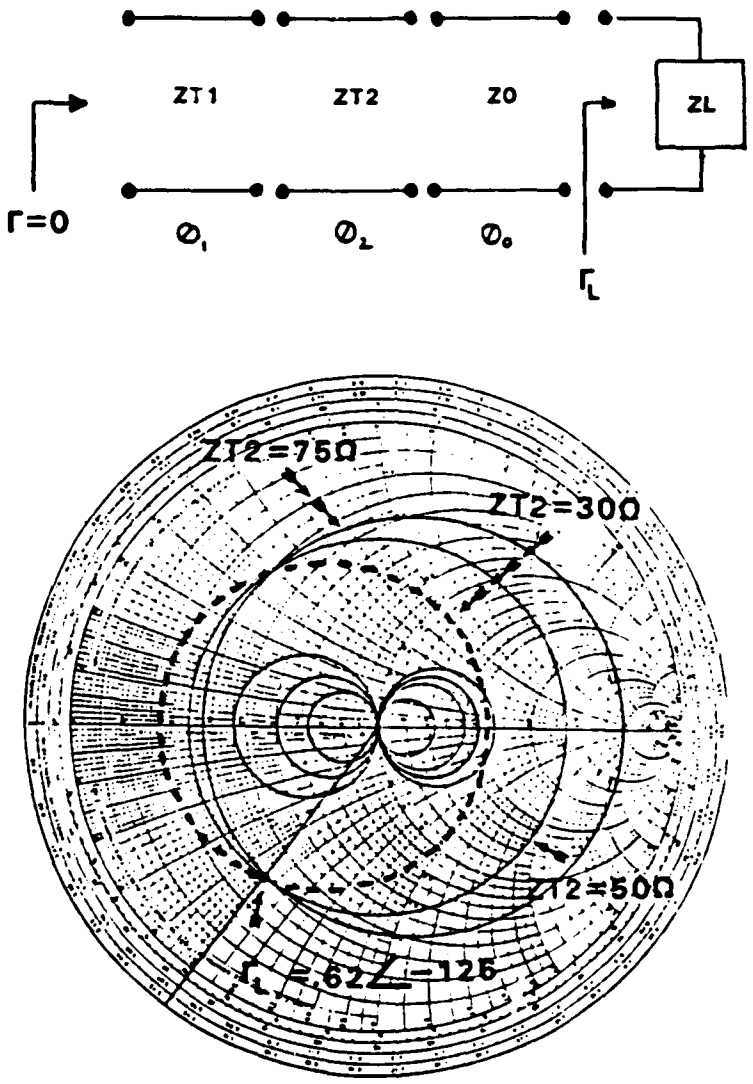


Figure 38. The Dual-section Matching Technique and a Smith Chart Example of Matching a Complex Load to Z_O Ohms Using the Technique

If ZT2 is less than Z_O, the centers of the circles are located to the left of the center of the Z_O Smith chart. If ZT2 is greater than Z_O, the centers are located to the right of the center of the Z_O Smith chart. As circles are plotted for higher values of the reflection coefficient on a ZT2 impedance line, the radius of the circle increases and the center moves toward the center of the Z_O Smith chart. Finally, at a reflection coefficient of a magnitude of one on any impedance ZT2 line,

the center of the circle is the center of the Smith chart and the radius is equal to one. In order to match a load impedance Z_L to Z_O Ω, a circle representing impedance transformation along ZT2 must pass through the point Γ_L, and the circle must intersect one of the quarter-wave transformer circles. Because the center of the ZT2 circle is offset from the center of the Smith chart, it will intersect different quarter-wave transformer circles than the same load transformed along a Z_O-Ω transmission line. If ZT2 < Z_O, the impedance transformation circle for ZT2 will intersect lower impedance values of quarter-wave transformer circles than those interested by the same load transformed along a Z_O-Ω line. IF ZT2 > Z_O, the opposite is true; the quarter-wave circles intersected by impedance transformation along the ZT2 line will represent higher impedance values than those intersected by transforming the load along a Z_O-Ω line.

Figure 38 also shows the matching of a $\Gamma_L = 0.62 < -126°$ using the dual-section technique. The circle representing a ZT2 section of 30 Ω passes through the load and also intersects the ZT1 circle for a 75-Ω impedance. A length of Z_O line could also be used with a shorter length of 30 Ω and a shorter length of 75 -Ω line.

The maximum magnitude of a reflection coefficient in the Z_O system than can be matched using a section of impedance ZT1 and a section of impedance ZT2 is easily derived from Smith chart considerations. Figure 39b depicts a Smith chart representation of a dual-section matching circuit using a ZT1 of 30 Ω and at ZT2 of 70-Ω. Two circles of constant reflection coefficient are plotted for the ZT2 line. The maximum reflection coefficient that can be matched is at the point $\bar{X}2$ on the real axis. The $\bar{X}2$ points on the Smith chart that represent the highest magnitude reflection coefficient that can be matched for all possible values of $\overline{ZT1}$ and $\overline{ZT2}$ are shown in Figure 39a. A combination of a $\overline{ZT1}$ 1.0 and a $\overline{ZT2}$ < 1.0 or vice-versa will match the highest magnitude reflection coefficient when the ZT2 circle intersects the ZT1 circle at the point of the ZT1 circle farthest from the center of the Smith chart. Each section will have an electrical length of 90°. The maximum magnitude of the reflection coefficient is easily derived. For the point $\bar{X}2$,

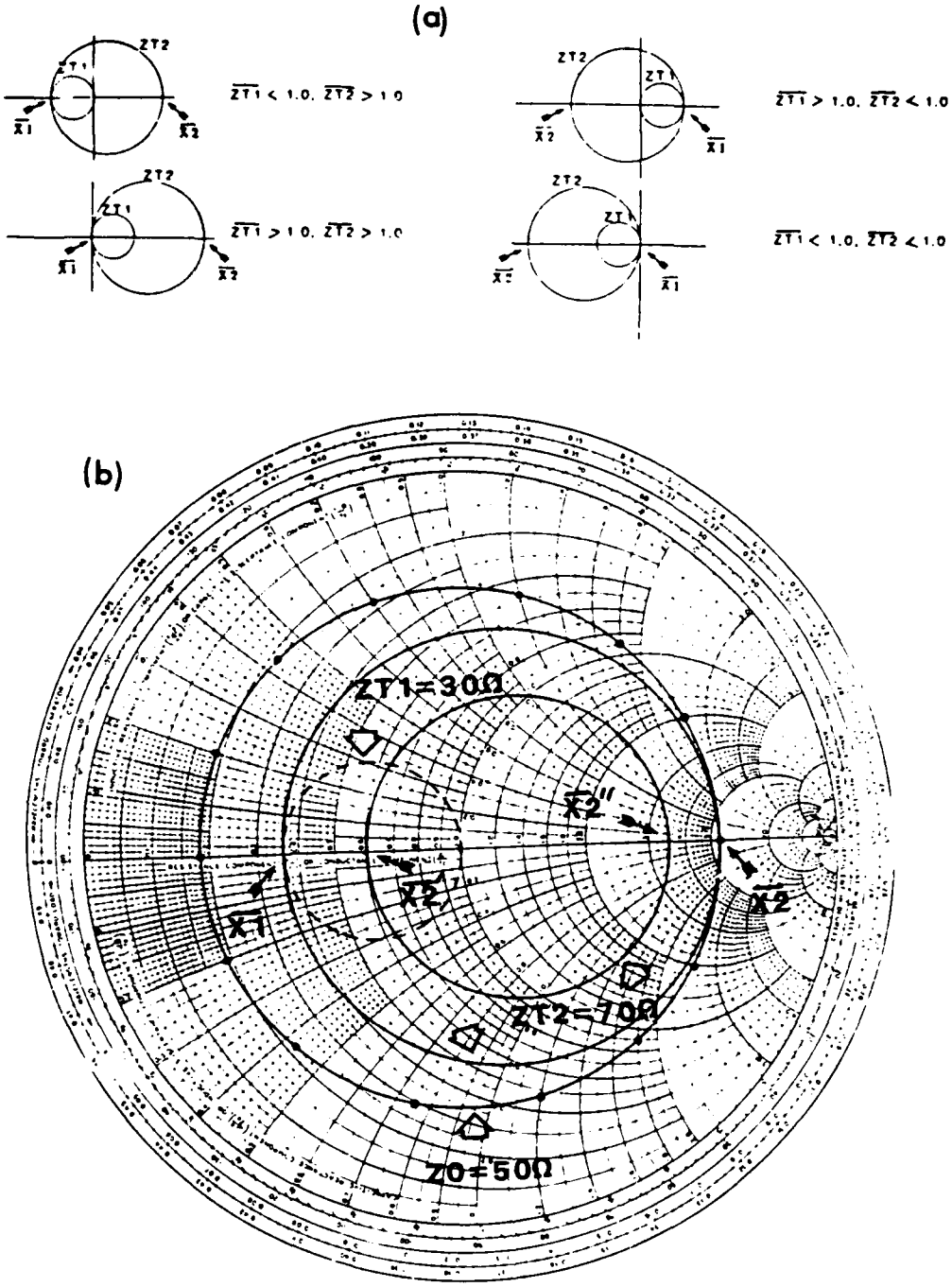


Figure 39. Graphs for Use in Derivation of Maximum Magnitude Reflection Coefficient That can be Matched to Z_O Ohms Using the Dual-section Method. Points marked "X2" represent the highest magnitude reflection coefficient that can be matched to Z_O ohms for the matching network shown

$$|\Gamma| = |\Gamma|_{max} = \frac{|\bar{X}2 - 1|}{|\bar{X}2 + 1|} \tag{46}$$

$$(\bar{X}2 \cdot \bar{X}1)^{1/2} = \bar{Z}T2 \tag{47}$$

$$(\bar{X}1)^{1/2} = \bar{Z}T1 \tag{48}$$

$$\bar{X}2 = \bar{Z}T2^{2} / \bar{Z}T1^{2} \tag{49}$$

$$|\Gamma|_{max} = \frac{|\bar{Z}T2^{2} - \bar{Z}T1^{2}|}{\bar{Z}T2^{2} + \bar{Z}T1^{2}} \qquad \begin{matrix} \bar{Z}T1 > 1.0,\ \bar{Z}T2 < 1.0 \\ \text{or} \\ ZT1 < 1.0,\ ZT2 > 1.0 \end{matrix} \tag{50}$$

Interchanging a $\overline{ZT1}$ and $\overline{ZT2}$ does not change the value of $|\Gamma|$ max. A $\overline{ZT1}$ of 0.6 and a $\overline{ZT2}$ of 1.2 will match the same maximum magnitude reflection coefficient as a $\overline{ZT1}$ of 1.2 and a $\overline{ZT2}$ of 0.6. Contours of constant $|\Gamma|$ max for the expression above and a Z_O of 50 Ω are plotted in Figure 40. Note that for a fixed range of available transmission line impedances, the dual-section technique allows a higher magnitude of the load reflection coefficient to be matched to 50 Ω than the single-technique. If $\overline{ZT1}$ and $\overline{ZT2}$ are both less than one or both greater than one, Figure 39 shows that the maximum magnitude of reflection coefficient is given by the limit of the single-section method using the value of $\overline{ZT1}$ or $\overline{ZT2}$ that is further from 1.0. There is no advantage, in terms of matching the highest magnitude reflection coefficient possible, in using a dual-section technique rather than a single-section method if both $\overline{ZT1}$ and $\overline{ZT2}$ are greater or less than one.

The author wrote two computer programs in FORTRAN to aid in using the dual-section matching technique. The first program, called CIRCLES2, was used to plot on the Smith chart the appropriate circles representing impedance transformation along the transmission line sections of impedance ZT1 and ZT2. Required as input were the reflection coefficient of the load to be matched, the value of Z_O, and stop, start, and step size values for the range of transmission line impedances to be considered for ZT1 and ZT2. The program calculated the centers and radii of the circles representing the ZT1 sections, and the centers and radii of circles that passed through the point Γ_L and represented impedance transformation along the ZT2 sections. A plot of these circles on the Smith chart provided at a glance an idea of the various dual-section networks that could be used to impedance match a Γ_L to Z_O Ω. The second program, named DUALM, used the same input data as CIRCLES2, but calculated directly the impedances and the electrical lengths of the ZT1 and ZT2 sections that could be used to match a given Γ_L to Z_O Ω. The program provided starting values to be used for optimization on SUPERCOMPACT®.

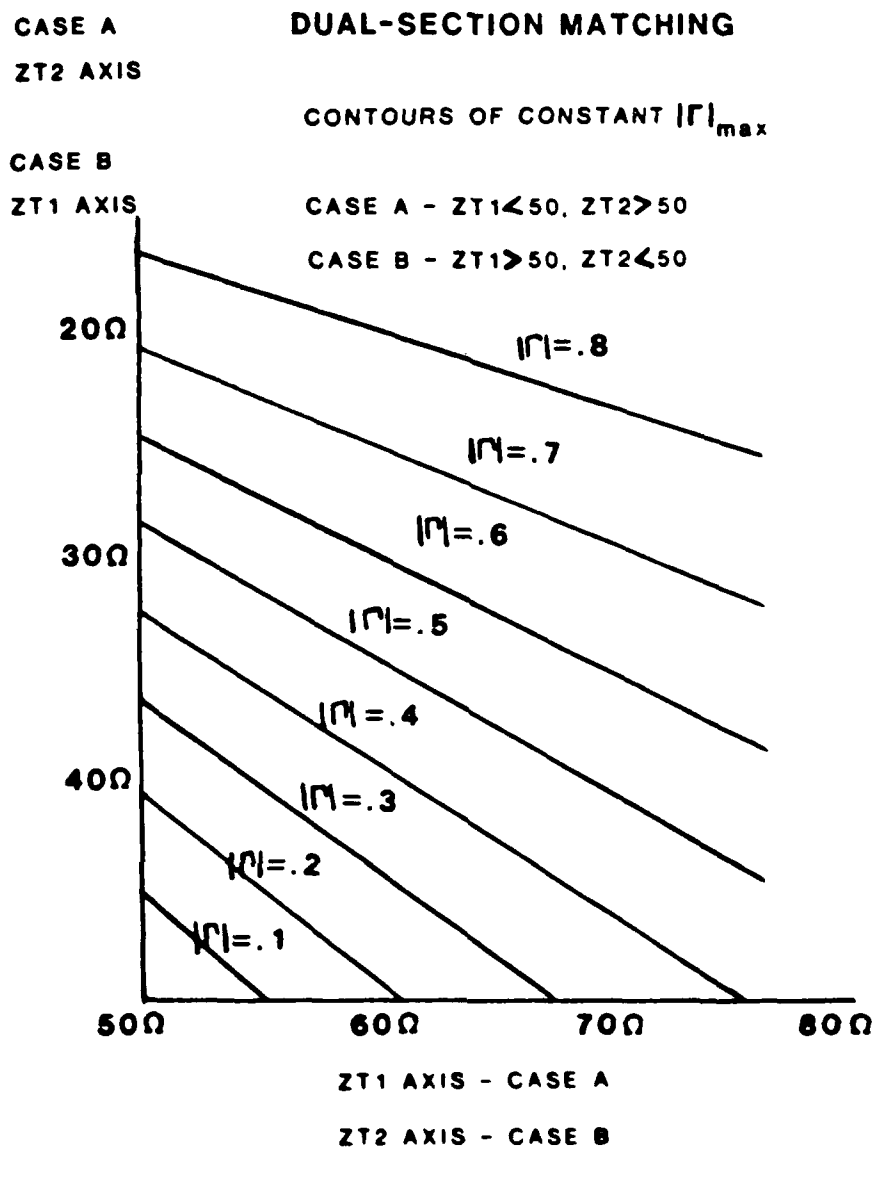


Figure 40. Contours of Constant Maximum Magnitude Reflection Coefficient That Can be Matched to 50 Ω Using the Dual-section Matching Technique

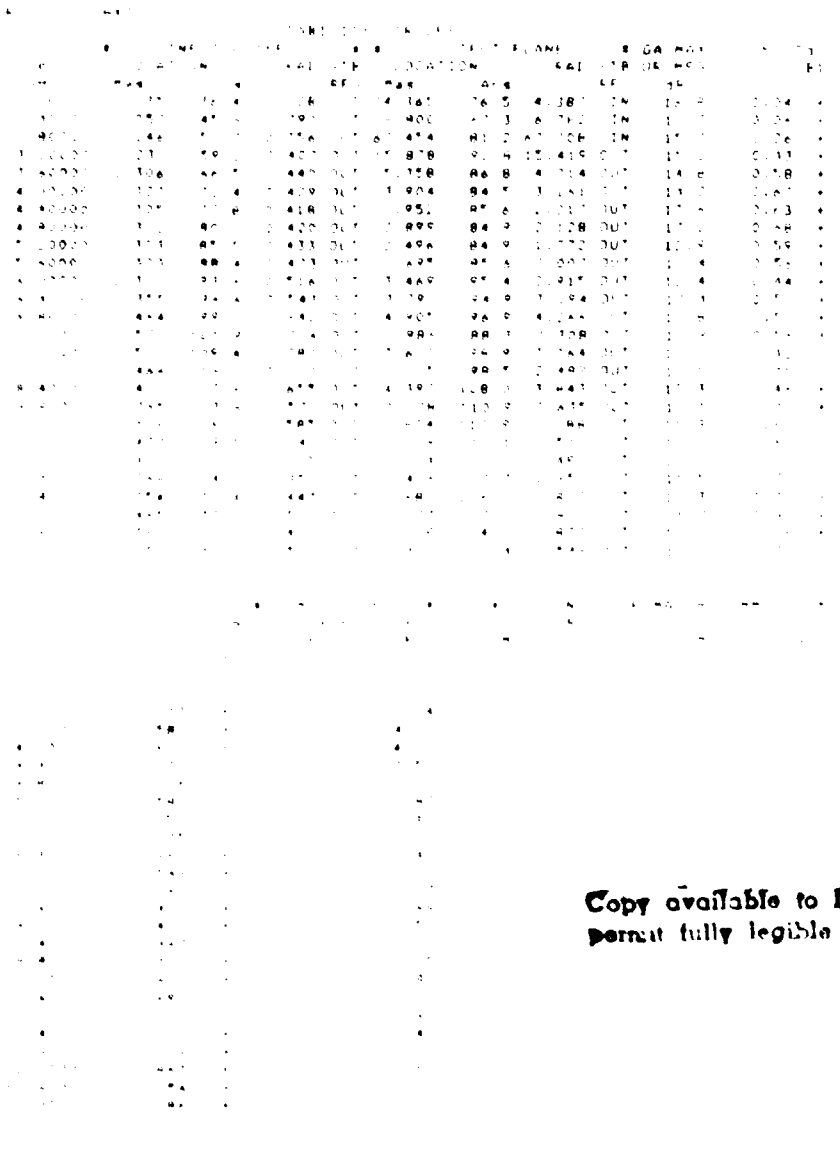
5.4 10 GHz Amplifier Design

5.4.1 CHOOSING Γ_S AND Γ_L

Table 2 lists the values of K and of the MSG [illegible] from an average of the de-embedded [illegible] that K is less than one, B_1 is positive and [illegible] tially unstable over the entire frequency range [illegible] use the MSG, the input and output stabil[illegible] power gain circles. Table 2 also [illegible]

the input and output stability circles for the averaged s-parameters, and some of these circles are plotted on Smith charts in Figure 41. As the frequency increases, the circles tend to move counterclockwise around the Smith chart, and to occupy less area on the chart. Although K is still less than one even at 12 GHz, stability analysis was not performed above this frequency. The circles are approaching the outer edges of the chart, and it is unlikely that an input or output matching network would present a reflection coefficient large enough to fall into either one of the circles.

Table 2. Locations of Stability Circles, Value of K-factor, and MSG Calculated From an Average of the De-embedded S-parameters of FETX and FETZ at an Ids of 30 mA. Data used for 10 GHz amplifier design



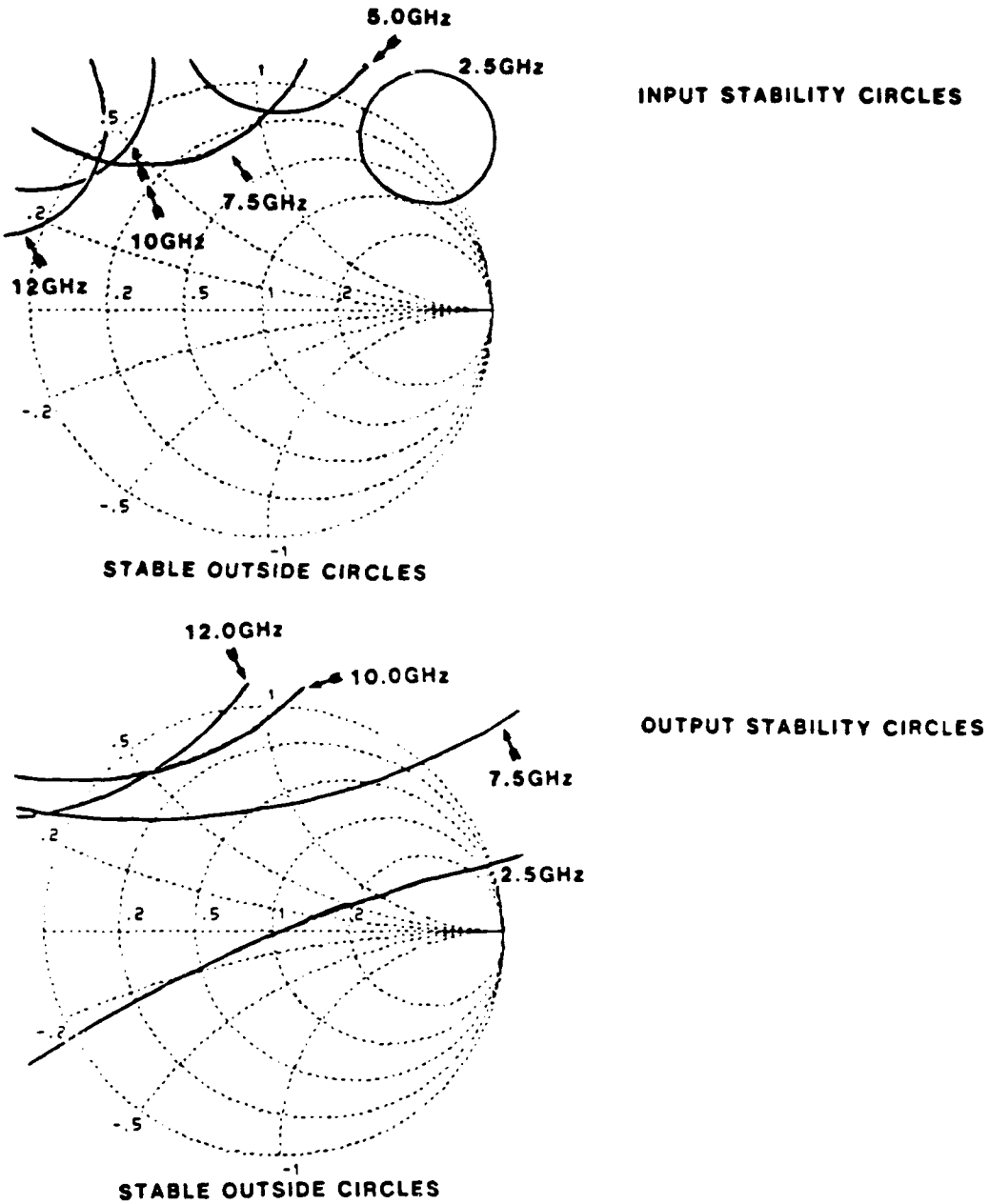


Figure 41. Input and Output Stability Circles Calculated From Averaged FETX and FETZ De-embedded s-parameters, Plotted for Selected Frequencies

From Table 2, the MSG at 10 GHz is 11.67 dB. An amplifier design that provides a gain equal to the MSG at 10 GHz would require Γ_S and Γ_L to lie on the boundary of the input and output stability circles, respectively. This approach is not advisable because uncertainties in the de-embedded s-parameters or in the actual behavior of the final, etched matching circuit may cause Γ_S and Γ_L to lie in the unstable region of a stability circle. Designing an unconditionally stable amplifier

would have added to the fabrication problems. Instead, it was decided to simply keep Γ_S and Γ_L a "safe" distance on the Smith chart from the appropriate stability circles. A "safe" distance was determined by examining the variation in the stability circles calculated from the de-embedded s-parameters of FETX, FETY, and FETZ. A Γ_S, for example, was not used if there was any possibility, given the magnitude of uncertainty on the location of the stability circles, that the Γ_S may actually be inside the unstable region of the circle. In this approach, it is not possible for the amplifier to have a gain equal to the MSG. Some gain must be sacrificed. Generally, the farther a Γ_S or Γ_L is from its stability circle, the less the transducer gain will be. At this point, the design basically involved finding a Γ_S and Γ_L that were an adequate distance from the stability circles, that gave as high a transducer gain as possible, and that could easily be matched to 50 Ω using series transmission line elements. As discussed in Section 5.4.2, in order to create matching networks using series CPW transmission lines only, the magnitudes of Γ_S and Γ_L had to be as small as possible.

Four available gain and four power gain circles were calculated on SUPERCOMPACT® from the averaged s-parameters of FETX and FETZ. These circles corresponded to values of the transducer gain ranging from 11.5 dB to 10.5 dB, in steps correspond of 0.5 dB. To determine a suitable Γ_S and Γ_L, each of the gain circles was plotted on a Smith chart, along with the 10 GHz input and output stability circles. Three or four points on each conjugate match locus were plotted, and the 0.5 dB and 1.0 dB mismatch circles corresponding to one point on each gain circle were also plotted. The four available gain circles are shown in Figures 42a and 42b and the four power gain circles are shown in Figures 43a and 43b.

There literally exists an infinite number of combinations of input and output reflection coefficients that may be presented to the active device to achieve a transducer gain that is less than the MSG (MAG, if it exists). For a transducer gain of G dB where G < MSG, any of the following four methods will work:

(1) Choose any Γ_S on the Available Gain = G dB circle, and use the appropriate Γ_L for conjugate match at the output.

(2) Choose any Γ_L on the power gain = G dB circle, and use the appropriate Γ_S for conjugate match at the input.

(3) Choose any Γ_S on the available gain = G + ΔG dB circle. Find the appropriate ΔG dB mismatch circle corresponding to the Γ_S. Choose any Γ_L on the ΔG dB mismatch circle.

(4) Choose any Γ_L on the power gain = G + ΔG dB circle. Find the ΔG dB mismatch circle corresponding to the Γ_L. Choose any Γ_S on the ΔG dB mismatch circle.

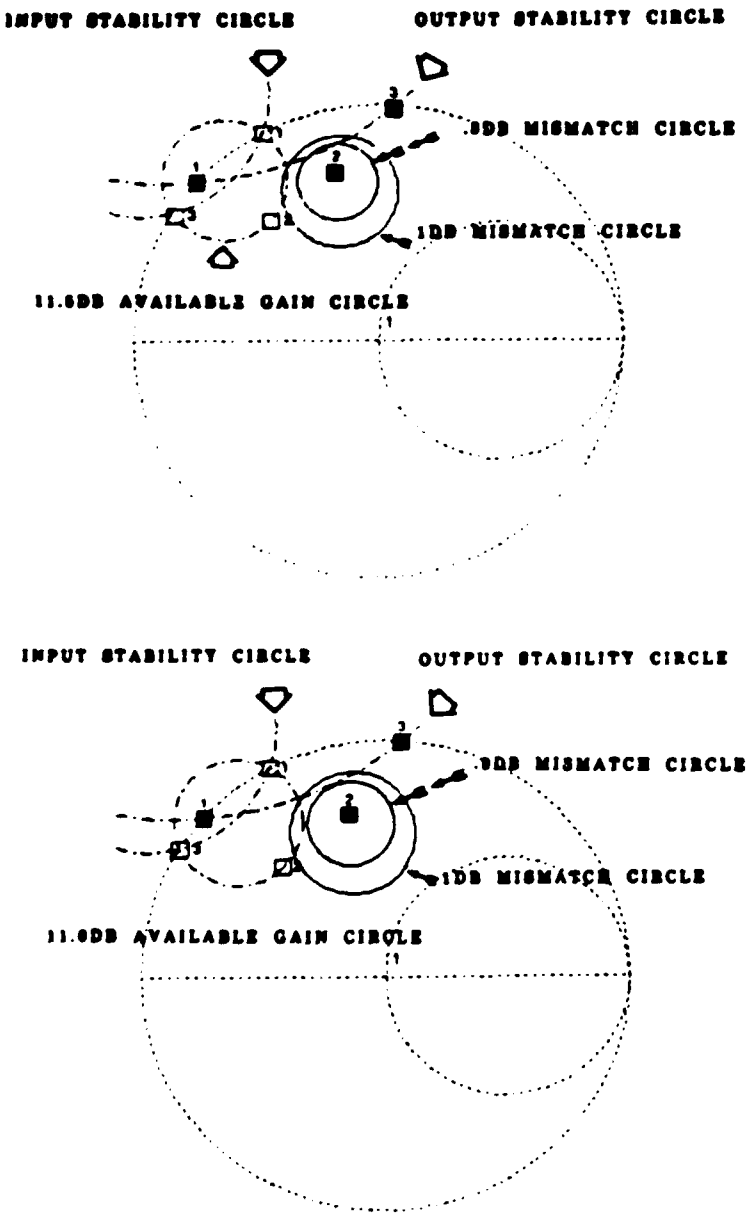


Figure 42a. 11.5 dB and 11.0 dB Available Gain Circles, 10 GHz Input and Output Stability Circles, and 1 dB and 0.5 dB Mismatch Circles Used for 10 GHz Amplifier Design

All amplifier designs using one of the methods on the preceding page to choose Γ_S and Γ_L will produce the same transducer gain at the design frequency. However, each method could produce a different match at both the input and output of the amplifier. If specifications exist for either Γ_S or Γ_L or the S_{11} or S_{22} of the amplifier, then, of course, these must be considered in a choice of

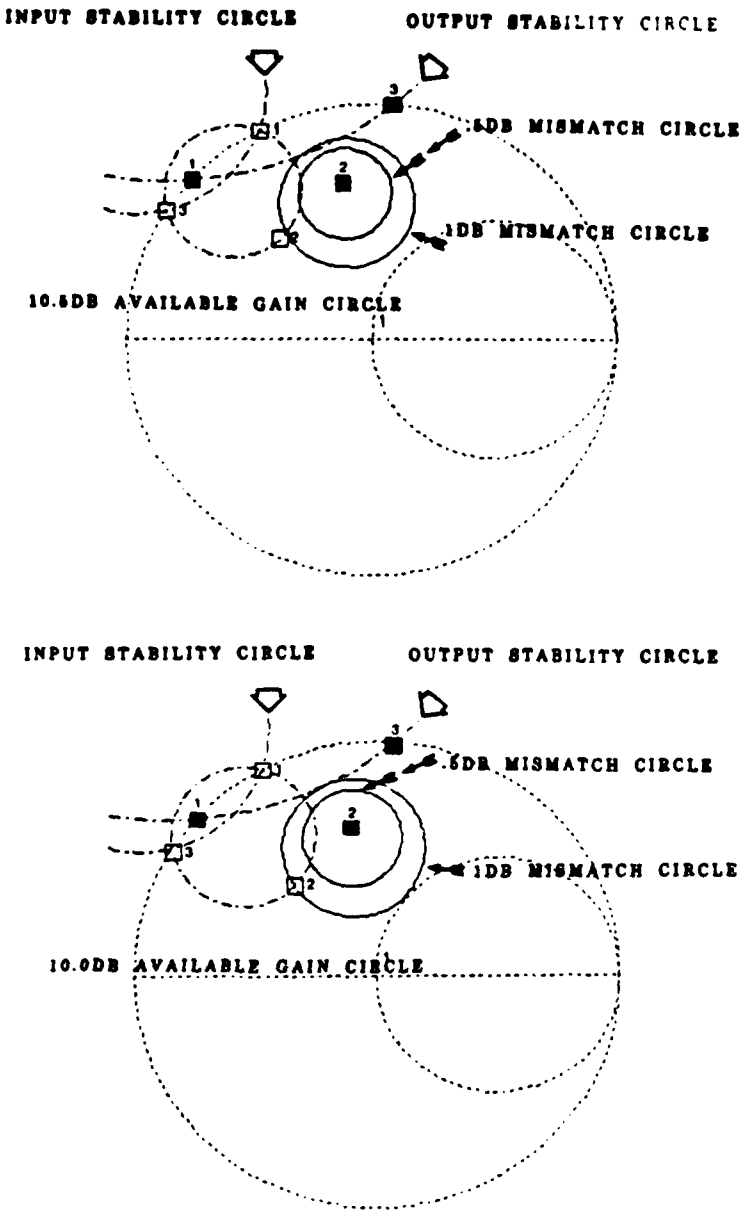


Figure 42b. 10.5 dB and 10.0 dB Available Gain Circles, 10 GHz Input and Output Stability Circles, and 1 dB and 0.5 dB Mismatch Circles Used for 10 GHz Amplifier Design

Γ_S and Γ_L. In this project, neither the input match nor the output match was required to be of a particular value. Stability was the major concern.

The eight plots in Figures 42 and 43 were used to determine the highest transducer gain that could be obtained using a Γ_S and Γ_L that were each an adequate distance from their respective stability circles. Full-size versions of the plots were overlaid on a light table, in order to see the various design trade-off in detail.

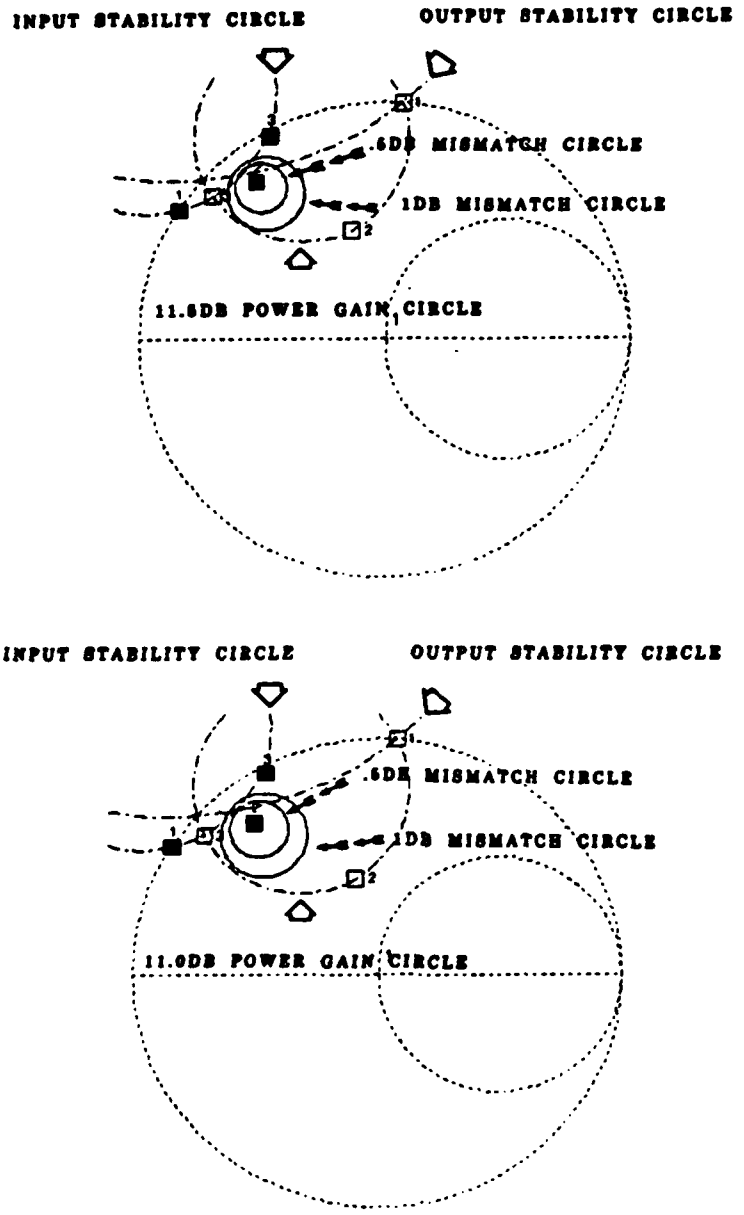


Figure 43a. 11.5 dB and 11.0 dB Power Gain Circles, 10 GHz Input and Output Stability Circles, and 1 dB and 0.5 dB Mismatch Circles Used for 10 GHz Amplifier Design

Fortunately, many of the infinite pairs of Γ_S and Γ_L that produced a given transducer gain could readily be seen to be poor choices or redundant. Neither method 1 nor method 2 proved to be very good for the purposes here. The reflection coefficient on the conjugate match circle was always too close to the appropriate stability circle. Methods 3 and 4 each produced a Γ_S and Γ_L that were more likely to be adequate distances from their respective stability circles. Although

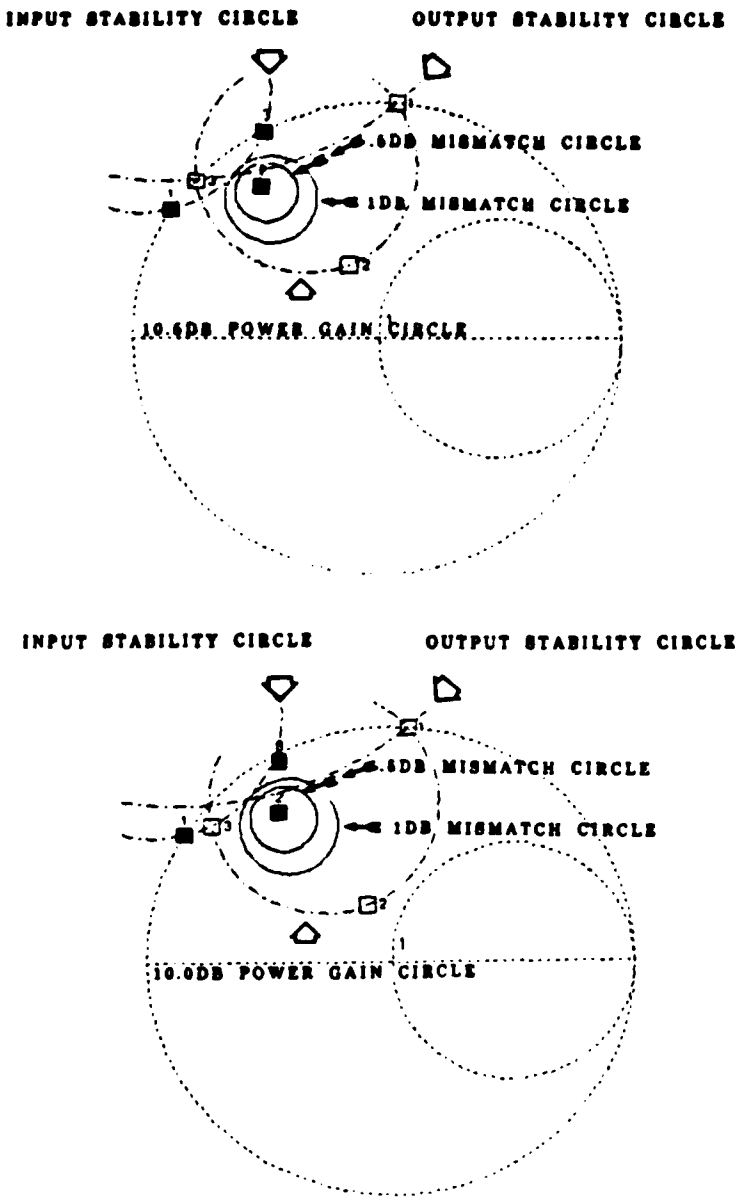


Figure 43b. 10.5 dB and 10.0 dB Power Gain Circles, 10 GHz Input and Output Stability Circles, and 1 dB and 0.5 dB Mismatch Circles Used for 10 GHz Amplifier Design

an infinite number of mismatch circles can be drawn, points on a given gain circle that were close to a stability circle produced mismatch circles that were near the opposite port's stability circle and had very small radii. The only points on a gain circle that produced useful mismatch circles were those that were far from the stability circles.

After careful study of the plots in Figures 42a through 43b, it was decided to design the amplifier for a transducer gain of 10.5 dB. Three pairs of Γ_S and Γ_L that will produce a transducer gain of 10.5 dB are shown in Figure 44. They are all very close to each other. The Γ_S and Γ_L used for the design were:

$\Gamma_S = 0.62 < 126°$

$\Gamma_L = 0.47 < 106°$

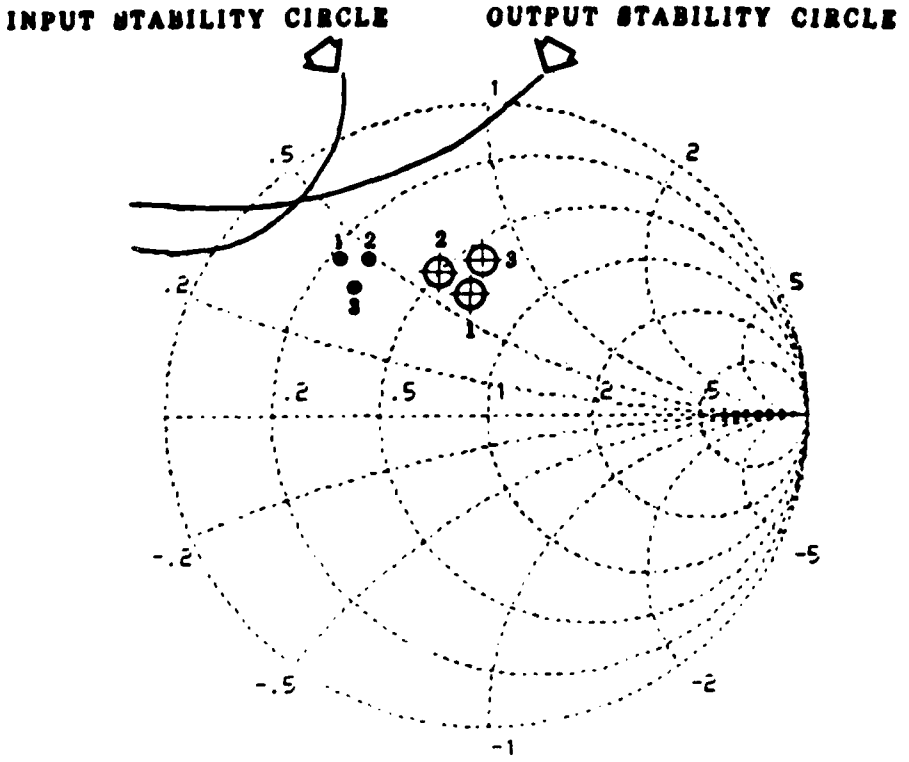


Figure 44. Three Source and Load Reflection Coefficients That Provide 10.5 dB Transducer Gain at 10 GHz

5.4.2 10 GHz MATCHING CIRCUIT DESIGN

The first matching circuits designed for the 10 GHz amplifier are shown in Figure 45. A single section design was attempted for the input and the output. The load impedances were rotated to the real axis of the Smith chart using sections of 50-Ω line, and then brought to the center of the chart using the standard quarter-wave transformer technique. The transformer impedance obtained in this manner are the closest to 50 Ω that the single-section matching technique will allow. The program SINGLEM.FOR was used to verify the Smith chart design.

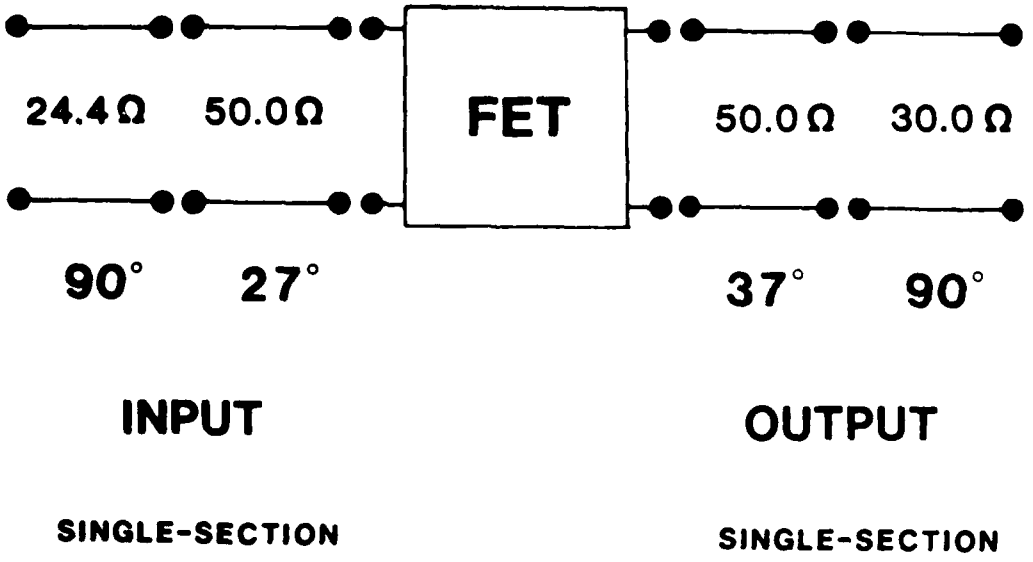


Figure 45. Initial Paper Design of 10 GHz CPW Amplifier. Electrical lengths of transmission lines are for a frequency of 10 GHz

Tables were generated using the TRL option of SUPERCOMPACT® to determine the various S and W CPW dimensions that produce 24.4 Ω and a 30-Ω characteristic impedance. Figures 46 and 47 were drawn to scale using these tables. A 50-Ω line of the dimensions used to accommodate the FET chips (S = 0.010 in., W = 0.007 in.) is included in each figure to indicate if a physical transition from each of the possible geometries to 50 Ω is feasible. Also included are a SUPERCOMPACT® analysis of the loss and a calculation to indicate the sensitivity of the impedance to slight dimension changes in the CPW line. The loss analysis was used for relative comparisons only, as the loss predictions of SUPERCOMPACT® were not found to agree well with the loss measured in the laboratory.

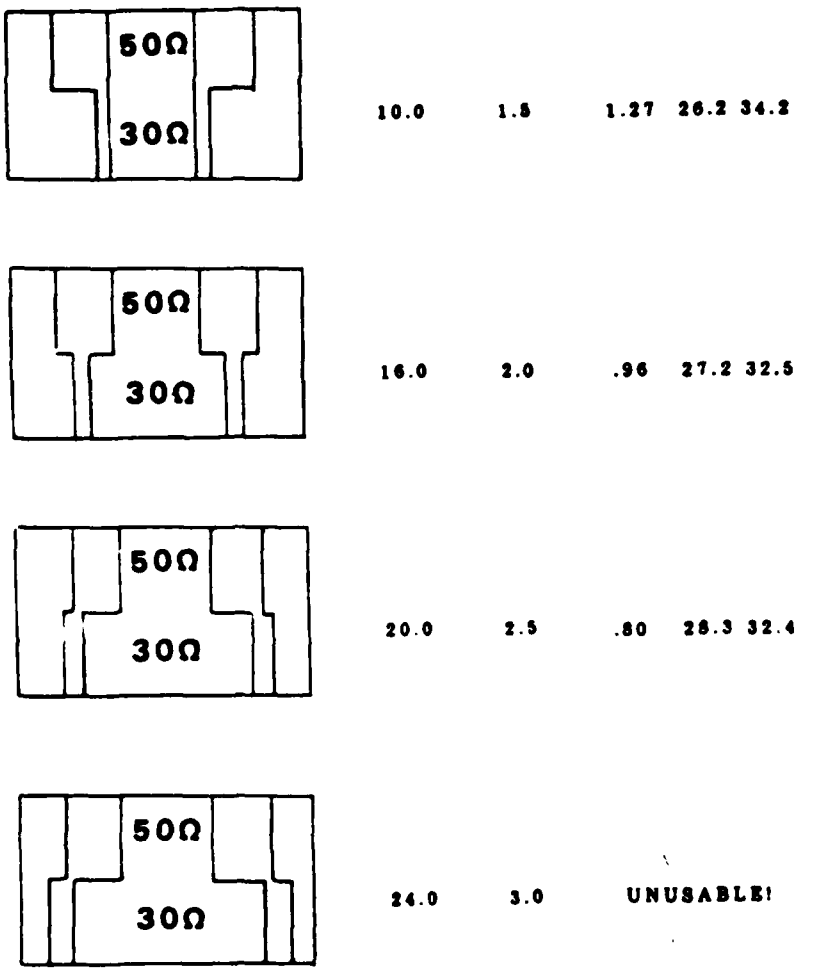


Figure 46. Various Configurations of 30-Ω CPW Transmission Lines. Loss and sensitivity to dimensional errors are both a function of the CPW S and W dimensions. Loss was calculated on SUPERCOMPACT® and is for comparison purposes only. Geometrical transition to 50-Ω CPW is included to give an idea of discontinuities

Many variables exist in the photolithography process, any one of which can have an effect on the final circuit dimensions. The right most columns in Figures 46 and 47 indicate the CPW impedance that would result for two cases of minor changes in the S and W dimensions of the CPW. An uncertainty of ± 0.00025 in. was assumed to exist in the position of any of the boundaries that define the CPW line. The characteristic impedance was examined for two cases - S + 0.0005 in., W - 0.0005 in. and S - 0.0005 in., W + 0.0005 inch.

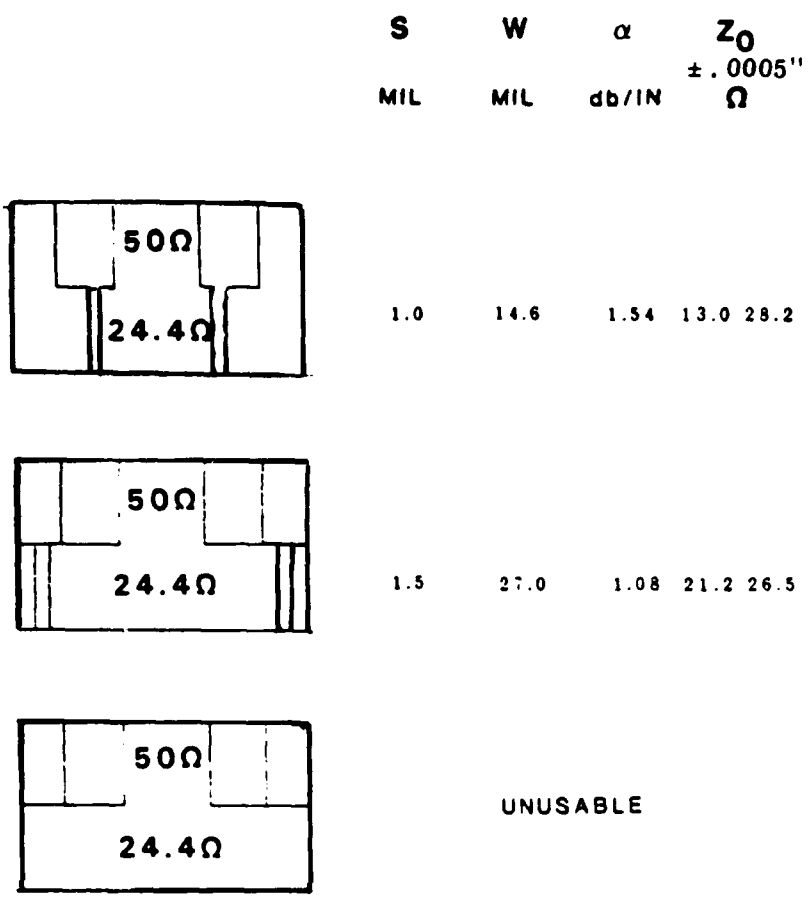
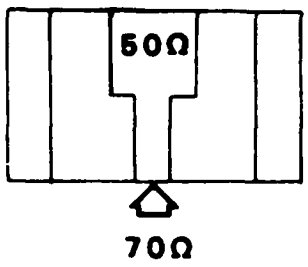


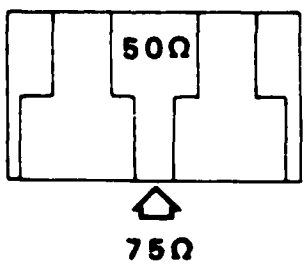
Figure 47. Various Configurations of 24.4-Ω CPW Line

In Figure 46, the third 30-Ω line from the top has lower loss than the first two and an S dimension that is reasonable. It was chosen as the best compromise. Unfortunately, the top 24.4-Ω line in Figure 47 has a sensitivity to dimension changes that is unacceptable. The bottom and middle 24.4-Ω lines have S dimensions that are larger than the S+ 2W dimension of the 50-Ω line. The author felt that 0.002 in. was the smallest size slot or line that should be used, due to possible problems with etching. This requirement eliminates the middle 24.4-Ω line as a possibility. The bottom line in Figure 47, with a W dimension of 0.002 in., has an S dimension nearly twice the S+ 2W dimension of the 50-Ω line, to which it must be attached. A constant impedance taper could have been used to increase the size of the 50-Ω line and facilitate its connection to the 24.4-Ω line, but the Keff varies along the taper, making an exact knowledge of the phase shift introduced by the taper difficult. It was decided to use a dual-section matching network rather than the 24.4-Ω line to provide the proper Γ_S. The tables generated from SUPERCOMPACT® of CPW dimensions and impedances were consulted to

determine the highest impedance lines that could be fabricated. Figure 48 shows acceptable geometries for both 70 Ω and 75-Ω transmission lines. Figure 48, previously used in the discussion on dual-section matching, indicates that a 30-Ω line with a 75-Ω line will match a Γ_S of 0.62 < -126° to 50 Ω. A SUPERCOMPACT® file was written using the dual-section network on the input and the single-section circuit on the output. A short piece of 50-Ω line was included between the input terminals of the FET chip and the dual-section circuit to provide another variable that could be used by SUPERCOMPACT® to optimize the performance of the amplifier. A diagram of the optimized circuit, and the predicted amplifier performance are shown in Figures 49 and 50. A stability analysis of the active device s-parameters cascaded with the matching circuits indicated that the center of the Smith chart was in the stable region of all the stability circles. The amplifier should not oscillate into 50-Ω source and load impedances.



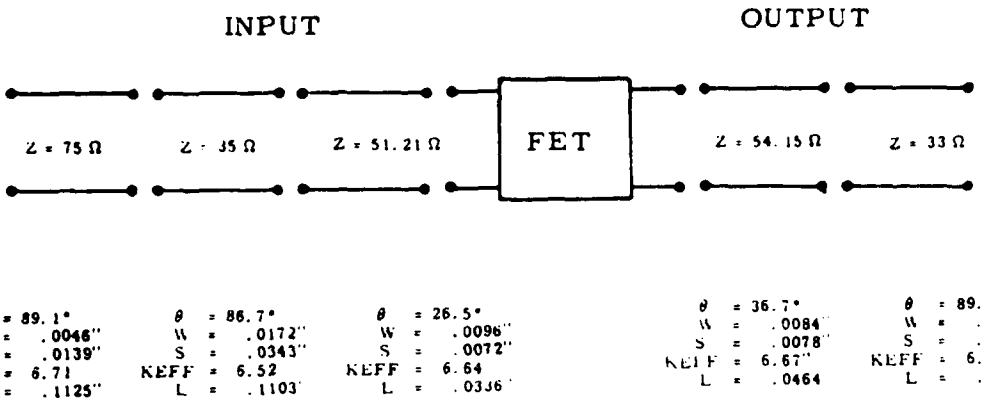
S	W	α	Z_0 ±.0005"	
MIL	MIL	db/IN	Ω	
4.0	10.0	.59	67.3	74.0



4.6	13.9	.47	72.7	78.3

Figure 48. Possible Configurations of 70-Ω and 75-Ω CPW Lines

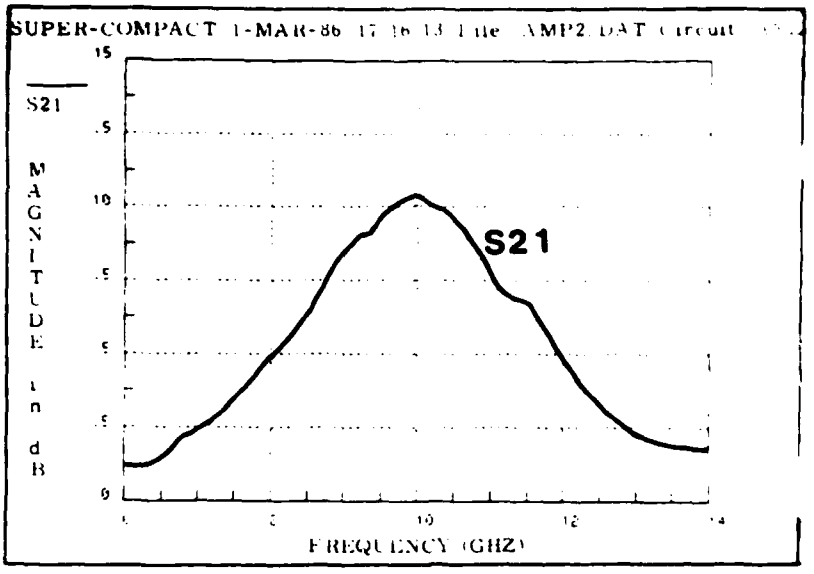
FINAL 10GHz AMPLIFIER DESIGN



DUAL-SECTION AND SINGLE-SECTION

Figure 49. Final 10 GHz CPW Amplifier Design. Electrical lengths of transmission lines are for a frequency of 10 GHz

A design with dual-section matching networks on the input and output did not provide any better performance. The design in Figure 49 was used for the 10 GHz amplifier, and the bottom of the figure indicates the exact CPW dimensions used. All the Keff and impedance values used on the final design were designed from SUPERCOMPACT®, and a few of them were checked using a program based on a full-wave analysis. No significant differences were found to exist between the full-wave analysis and SUPERCOMPACT® for a frequency of 10 GHz, and for the CPW geometries used on the 10 GHz amplifier design. It was assumed that the metallization on the substrates was 0.0001-in. thick and that the etching process was isotropic; therefore the dimensions of all lines and slots on the mask were adjusted to compensate for 0.0001 in. overetching. The dimensions of the final circuits were within 0.0005 in. of those of the design. Advanced Reproductions of North Andover, MA fabricated the mask on a 2-1/2 in. × 2-1/2 in. glass plate from a set of 25-to-1 enlarged coordinates of the circuit. MPC, of Lowell, MA etched the circuits and Digital Dicing of Attleboro, MA diced and grooved the substrates.



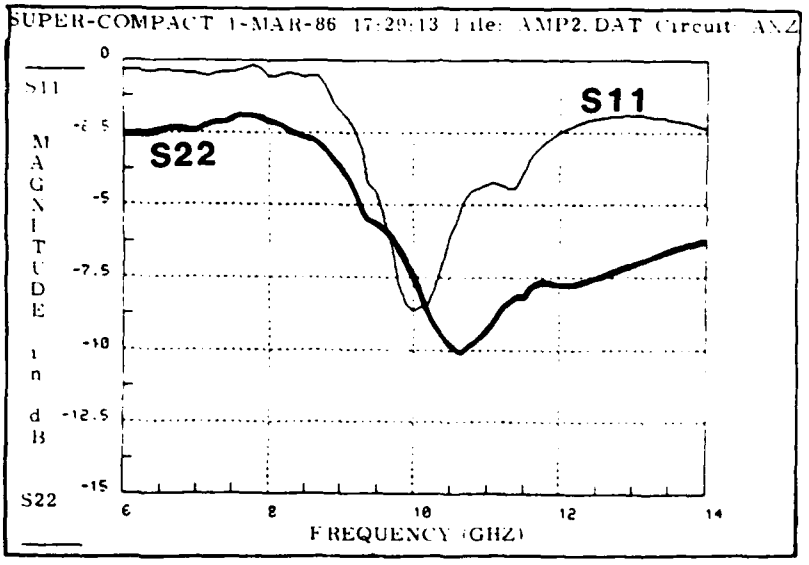


Figure 50. SUPERCOMPACT® Prediction of 10 GHz CPW Amplifier Performance, Using Design in Figure 49

5.4.3 PERFORMANCE OF 10 GHz AMPLIFIERS

Two identical 10 GHz amplifiers, AMP1 and AMP2, were built. An assembled 10 GHz amplifier is pictured in Figure 51 as well as an enlargement of the photomask. Figure 52 shows the gain of the two amplifiers, as measured on an HP 8409 automatic network analyzer. In Figures 52a and 52b the $|S_{11}|$ and $|S_{22}|$ of each of the amplifiers is plotted, and Table 3 lists the s-parameters of each of

the amplifiers. AMP1 had a maximum gain of approximately 8.4 dB, AMP2 had a maximum gain of approximately 10 dB.

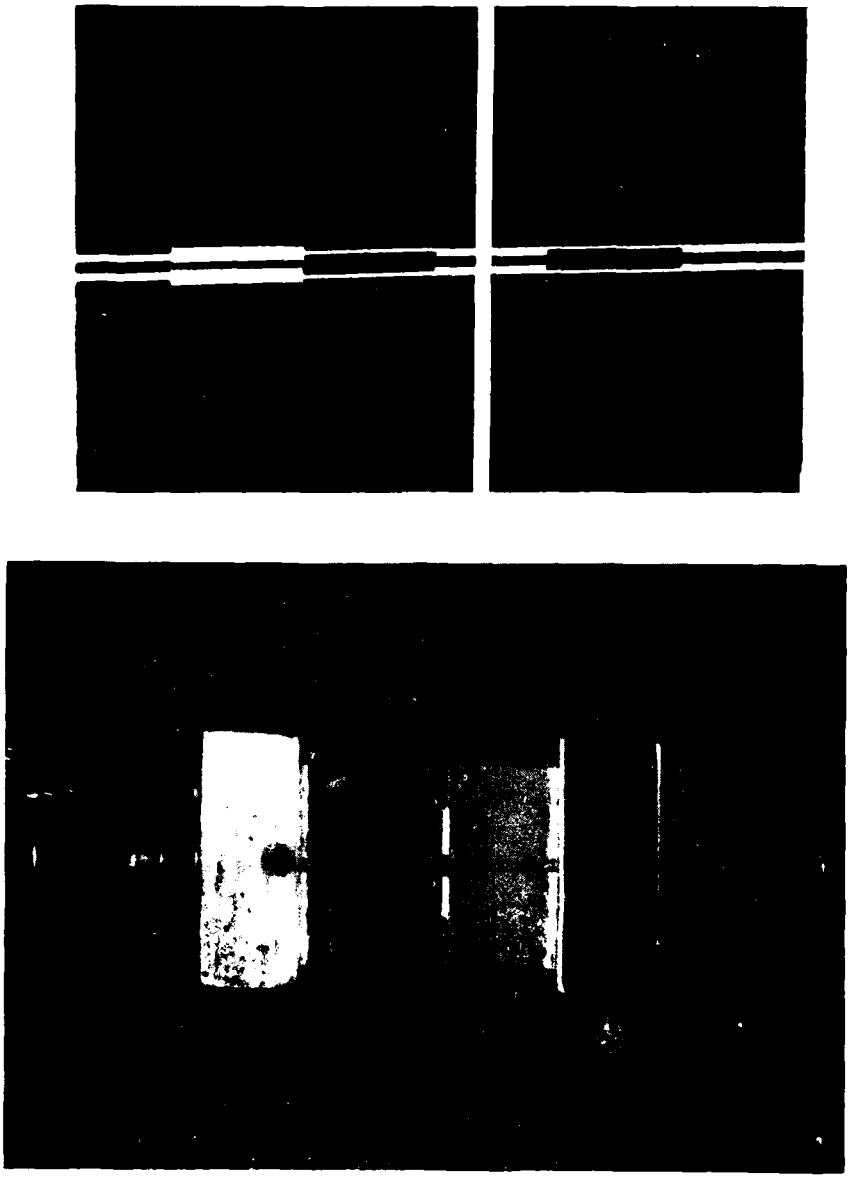


Figure 51. Enlargement of 10 GHz Amplifier Microstrip Circuit Prototype Showing [illegible] 10 GHz GaAs Amplifier

AD-A182 751 NARROWBAND 10 GHZ AND 20 GHZ GAAS FET AMPLIFIERS IN COPLANAR WAVEGUIDE(U) ROME AIR DEVELOPMENT CENTER GRIFFISS AFB NY P J RAINVILLE OCT 86 RADC-TR-86-169 2/2

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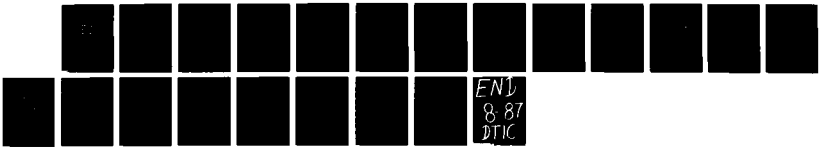

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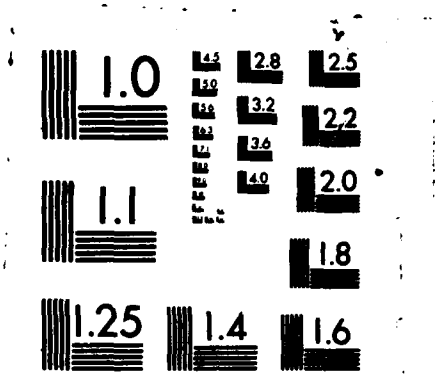


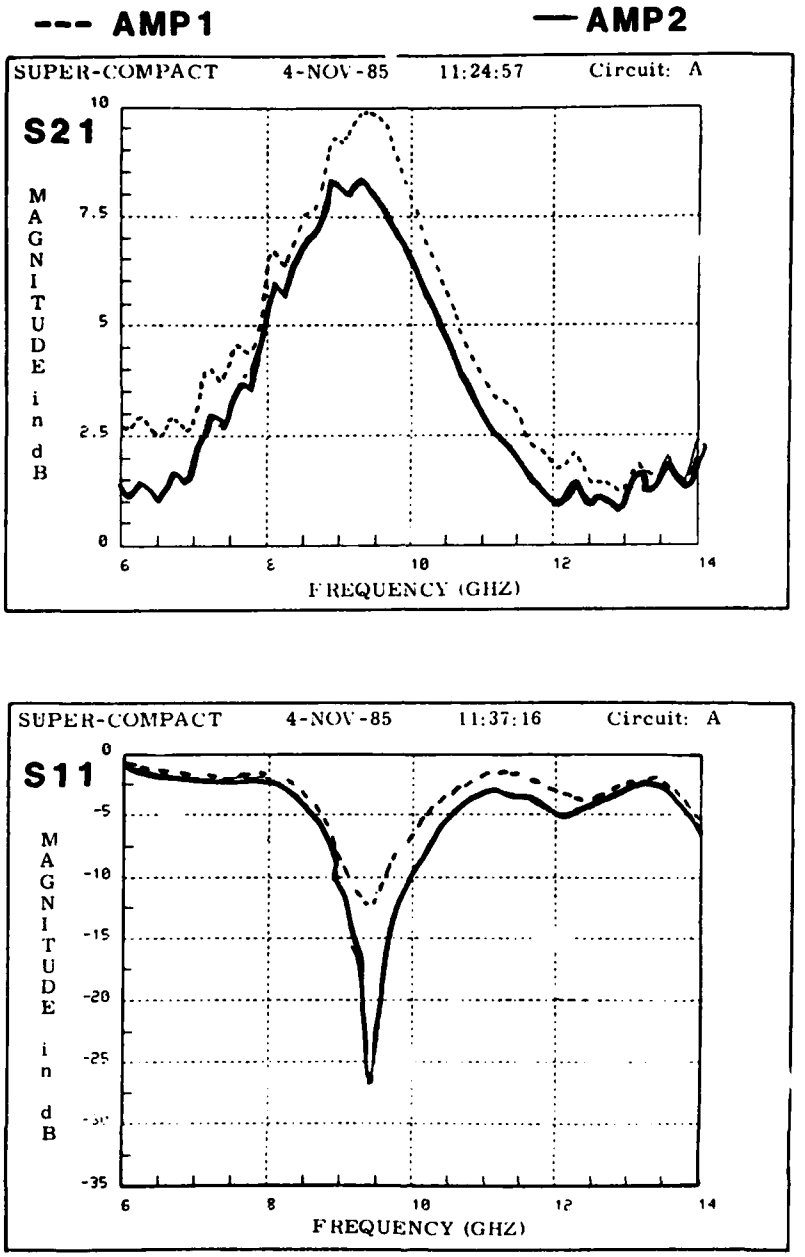


Figure 52a. S_{21} and S_{11} of Assembled 10 GHz CPW Amplifiers

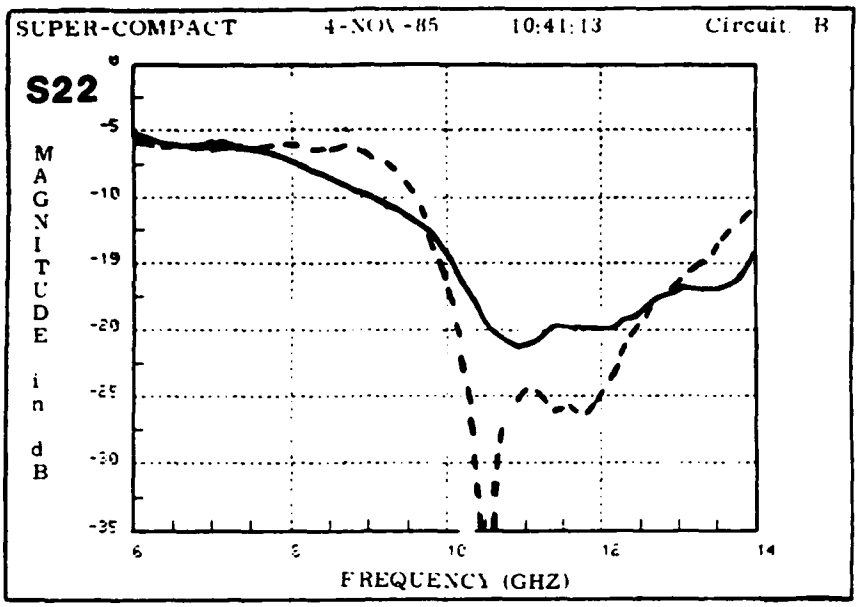


Figure 52b. S_{22} of Assembled 10 GHz CPW Amplifiers

The maximum gain of both AMP1 and AMP2 occurred at approximately 9.3 GHz—7 percent lower than the 10 GHz design goal. This is most probably due to the discontinuities between the transmission sections of different impedances. A first-order electrical model of the discontinuities is a small parallel capacitor placed at each junction where two different impedance transmission lines meet. The capacitor will, in many cases, have the same effect on overall circuit performance as a slight increase in the length of the transmission line sections. SUPERCOMPACT® was used to qualitatively determine the effect of these models of the discontinuities on the amplifier performance. Adding small parallel capacitors or increasing the length of the transmission line sections was found to shift the gain peak of the amplifier to a lower frequency.

It occurred to the author that it was possible, using gold ribbon and the bonding machine, to decrease the electrical length of the 75-Ω transmission line on the actual amplifier. SUPERCOMPACT® analysis indicated that reducing the length of the 75-Ω line from 0.115 in. to 0.075 in. should help the gain peak to near 10 GHz. Different lengths of 0.010 in. wide gold ribbon were bonded on the AMP2 75-Ω line in the manner indicated in Figure 53. After several trips between the bonding machine and the network analyzer, a length 0.060 in. was found to work the best. Any gap between the ribbon and the D-13 would lower the Keff of the section of transmission line made with the ribbon. This may explain why a longer length of ribbon had to be bonded onto the circuit than predicted by SUPERCOMPACT.®

Table 3. S-parameters of the Two 10 GHz CPW Amplifiers, as Measured on an HP-8409 Network Analyzer Using an Eight-term Error Correction Routine

AMP 1

CIRCUIT: B
S-MATRIX, ZS = 50.0+J 0.0 ZL = 50.0+J 0.0

Freq	S11		S21		S12		S22		S21
GHZ	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang	dB
2.00000	1.200	-19.6	2.344	-145.1	0.065	139.6	0.742	-62.5	7.40
2.25000	1.183	-19.9	2.284	-145.4	0.065	139.3	0.728	-62.8	7.17
2.50000	1.165	-20.3	2.223	-145.8	0.065	139.0	0.715	-63.3	6.94
2.75000	1.147	-20.7	2.162	-146.1	0.065	138.6	0.701	-63.7	6.70
3.00000	1.129	-21.2	2.102	-146.6	0.065	138.2	0.688	-64.3	6.45
3.25000	1.111	-21.7	2.041	-147.1	0.065	137.7	0.674	-64.9	6.20
3.50000	1.093	-22.4	1.980	-147.7	0.065	137.1	0.660	-65.7	5.93
3.75000	1.075	-23.2	1.920	-148.5	0.065	136.4	0.647	-66.6	5.66
4.00000	1.057	-24.2	1.859	-149.4	0.065	135.5	0.633	-67.8	5.38
4.25000	1.040	-25.4	1.798	-150.6	0.065	134.3	0.620	-69.2	5.10
4.50000	1.022	-27.1	1.737	-152.2	0.065	132.8	0.606	-71.1	4.80
4.75000	1.004	-29.3	1.677	-154.3	0.065	130.8	0.592	-73.7	4.49
5.00000	0.986	-32.6	1.616	-157.4	0.065	127.8	0.579	-77.4	4.17
5.25000	0.968	-37.6	1.555	-162.2	0.065	123.1	0.565	-83.0	3.84
5.50000	0.950	-46.2	1.495	-170.5	0.065	115.0	0.552	-92.4	3.49
5.75000	0.932	-63.0	1.434	172.9	0.065	98.6	0.538	-109.5	3.13
6.00000	0.914	-96.4	1.373	138.6	0.065	63.2	0.524	-139.7	2.76
6.25000	0.896	-138.0	1.312	95.1	0.064	18.5	0.503	-175.3	2.82
6.50000	0.859	-179.3	1.333	49.7	0.060	-19.8	0.497	152.1	2.49
6.75000	0.831	139.4	1.493	7.1	0.069	-58.9	0.492	116.7	2.94
7.00000	0.818	97.9	1.457	-32.0	0.071	-97.7	0.493	79.0	2.65
7.25000	0.805	56.0	1.099	-79.9	0.087	-145.7	0.484	39.4	4.08
7.50000	0.815	13.1	1.593	-121.9	0.090	172.2	0.493	2.0	4.05
7.75000	0.819	-27.3	1.619	-169.7	0.097	125.2	0.496	-36.2	4.34
8.00000	0.822	-72.1	2.097	150.6	0.120	86.2	0.500	-77.9	6.13
8.25000	0.764	-115.6	2.078	95.9	0.125	32.1	0.476	-119.6	6.35
8.50000	0.672	-162.7	2.369	48.6	0.148	-13.5	0.475	-167.6	7.49
8.75000	0.564	149.2	2.539	1.8	0.163	-59.5	0.498	145.6	8.06
9.00000	0.370	90.3	2.912	-55.3	0.191	-117.7	0.450	97.9	9.29
9.25000	0.280	12.9	3.037	-106.2	0.206	-167.7	0.436	52.5	9.65
9.50000	0.246	-98.8	3.095	-165.4	0.213	135.4	0.360	2.6	9.79
9.75000	0.385	175.9	3.087	136.7	0.201	77.3	0.249	-51.6	9.13
10.00000	0.161	111.9	2.593	84.1	0.184	24.9	0.152	-92.2	7.93
10.25000	0.590	58.2	2.191	33.6	0.162	-21.5	0.067	-130.3	6.83
10.50000	0.671	11.1	1.995	-14.7	0.147	-72.0	0.006	131.9	5.78
10.75000	0.756	-32.2	1.792	-61.2	0.132	-117.3	0.046	13.3	4.62
11.00000	0.810	-72.4	1.578	-105.3	0.124	-160.8	0.058	-14.8	3.85
11.25000	0.839	-114.1	1.463	-148.8	0.117	157.8	0.056	-32.4	3.30
11.50000	0.812	-154.1	1.416	163.1	0.119	110.7	0.052	-54.5	3.02
11.75000	0.754	164.1	1.398	121.2	0.112	69.0	0.047	-87.9	2.20
12.00000	0.698	122.2	1.389	77.9	0.112	24.1	0.057	-120.4	1.90
12.25000	0.647	78.5	1.359	34.0	0.112	-18.4	0.079	-132.1	2.00
12.50000	0.659	36.6	1.350	-11.2	0.107	-66.7	0.106	-162.7	1.45
12.75000	0.686	-5.0	1.139	-57.4	0.106	-108.2	0.135	175.5	1.44
13.00000	0.759	-46.1	1.155	100.0	0.104	-151.0	0.152	149.2	1.26
13.25000	0.791	-86.7	1.280	-147.3	0.113	163.3	0.178	115.8	1.80
13.50000	0.777	-128.6	1.297	168.7	0.114	121.7	0.200	81.2	1.65
13.75000	0.675	-168.0	1.135	120.1	0.116	67.6	0.244	44.9	1.47
14.00000	0.516	150.4	1.256	76.8	0.119	29.5	0.299	18.0	2.00

Table 3. S-parameters of the Two 10 GHz CPW Amplifiers, as Measured on an HP-8409 Network Analyzer Using an Eight-term Error Correction Routine (Contd)

AMP2

TYAAUDIT.DAT

SUPER-COMPACT Version 1.7 # 001 04/09/84 21-MAY-86 10:54:39

CIRCUIT: A
S-MATRIX: ZS = 50.0+J 0.0 ZL = 50.0+J 0.0

Freq	S11		S21		S12		S22		S21
GHZ	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang	dB
2.00000	1.611	-29.1	2.327	-147.9	0.063	137.5	0.719	-55.1	7.34
2.25000	1.566	-29.4	2.255	-148.2	0.063	137.2	0.708	-55.5	7.06
2.50000	1.521	-29.7	2.184	-148.5	0.062	136.9	0.696	-55.9	6.78
2.75000	1.476	-30.1	2.112	-148.9	0.062	136.5	0.684	-56.4	6.49
3.00000	1.431	-30.6	2.040	-149.3	0.061	136.0	0.673	-57.0	6.19
3.25000	1.386	-31.1	1.968	-149.9	0.061	135.5	0.661	-57.8	5.88
3.50000	1.341	-31.8	1.896	-150.5	0.060	134.9	0.649	-58.6	5.56
3.75000	1.296	-32.6	1.824	-151.3	0.060	134.1	0.638	-59.6	5.22
4.00000	1.251	-33.6	1.752	-152.2	0.059	133.1	0.626	-60.9	4.87
4.25000	1.206	-34.9	1.680	-153.4	0.059	131.9	0.614	-62.5	4.51
4.50000	1.161	-36.5	1.608	-155.0	0.058	130.4	0.603	-64.6	4.13
4.75000	1.116	-38.8	1.536	-157.2	0.058	128.2	0.591	-67.4	3.73
5.00000	1.071	-41.9	1.465	-160.3	0.057	125.1	0.579	-71.4	3.31
5.25000	1.026	-46.3	1.393	165.2	0.057	120.6	0.568	-77.0	2.88
5.50000	0.981	-55.5	1.321	-173.6	0.056	111.4	0.556	-87.1	2.42
5.75000	0.936	-72.1	1.249	169.7	0.056	95.2	0.544	-104.2	1.93
6.00000	0.891	-105.8	1.177	135.5	0.055	60.7	0.533	-133.4	1.42
6.25000	0.857	148.1	1.171	93..	0.054	18.2	0.516	164.6	1.37
6.50000	0.837	120.5	1.138	49.9	0.054	12.4	0.502	145.1	1.35
6.75000	0.861	108.5	1.218	7.7	0.054	-11.9	0.497	134.5	1.71
7.00000	0.793	94.7	1.199	-31.8	0.053	-101.7	0.500	109.0	1.57
7.25000	0.794	64.1	1.300	-78.9	0.057	148.1	0.483	62.8	2.27
7.50000	0.835	1.5	1.170	-120.9	0.080	120.1	0.181	2.9	3.35
7.75000	0.796	-40.6	1.517	-168.9	0.090	123.7	0.471	-19.6	3.62
8.00000	0.795	-95.3	1.844	150.6	0.113	84.0	0.448	-51.3	5.31
8.25000	0.794	-126.9	1.926	95.8	0.118	29.6	0.408	-92.9	5.69
8.50000	0.841	-175.0	2.207	42.6	0.141	-17.4	0.368	-115.6	6.88
8.75000	0.892	139.3	2.251	-7.0	0.155	-66.1	0.360	158.2	7.04
9.00000	0.940	90.9	2.596	-59.1	0.174	-124.3	0.309	102.4	8.29
9.25000	0.951	37.1	2.589	-111.1	0.178	-175.3	0.303	17.8	8.26
9.50000	0.852	-156.3	2.526	-162.5	0.190	130.7	0.271	-8.7	8.05
9.75000	0.209	133.5	2.334	138.1	0.168	76.1	0.230	-65.8	7.36
10.00000	0.314	78.5	2.089	87.0	0.161	25.2	0.189	-110.9	6.39
10.25000	0.442	34.4	1.891	37.4	0.145	-23.5	0.144	-153.2	5.53
10.50000	0.540	-8.6	1.708	-10.2	0.136	-70.7	0.108	162.5	4.65
10.75000	0.629	-49.1	1.572	-57.6	0.125	-116.5	0.093	114.2	3.85
11.00000	0.679	-87.8	1.413	-101.7	0.120	-159.9	0.093	82.3	3.00
11.25000	0.695	-128.1	1.332	-146.1	0.116	156.2	0.102	60.8	2.51
11.50000	0.667	-168.3	1.264	166.5	0.114	109.5	0.107	41.5	2.04
11.75000	0.617	151.1	1.169	121.1	0.113	65.9	0.106	23.8	1.35
12.00000	0.571	111.2	1.139	81.5	0.112	18.3	0.102	-2.3	1.09
12.25000	0.581	67.1	1.171	33.3	0.102	-24.1	0.113	36.0	1.37
12.50000	0.617	23.0	1.116	-8.7	0.100	-65.6	0.116	-69.1	0.95
12.75000	0.664	-20.1	1.126	-53.8	0.103	-108.0	0.135	-103.7	1.03
13.00000	0.738	-61.1	1.130	-95.0	0.105	-149.9	0.150	-134.4	1.06
13.25000	0.754	-103.0	1.183	-144.4	0.114	162.8	0.153	-171.3	1.46
13.50000	0.720	-145.5	1.211	173.4	0.121	121.6	0.151	150.9	1.66
13.75000	0.578	174.3	1.169	127.4	0.123	77.1	0.159	100.2	1.35
14.00000	0.454	130.0	1.134	78.3	0.133	32.1	0.217	48..	1.09

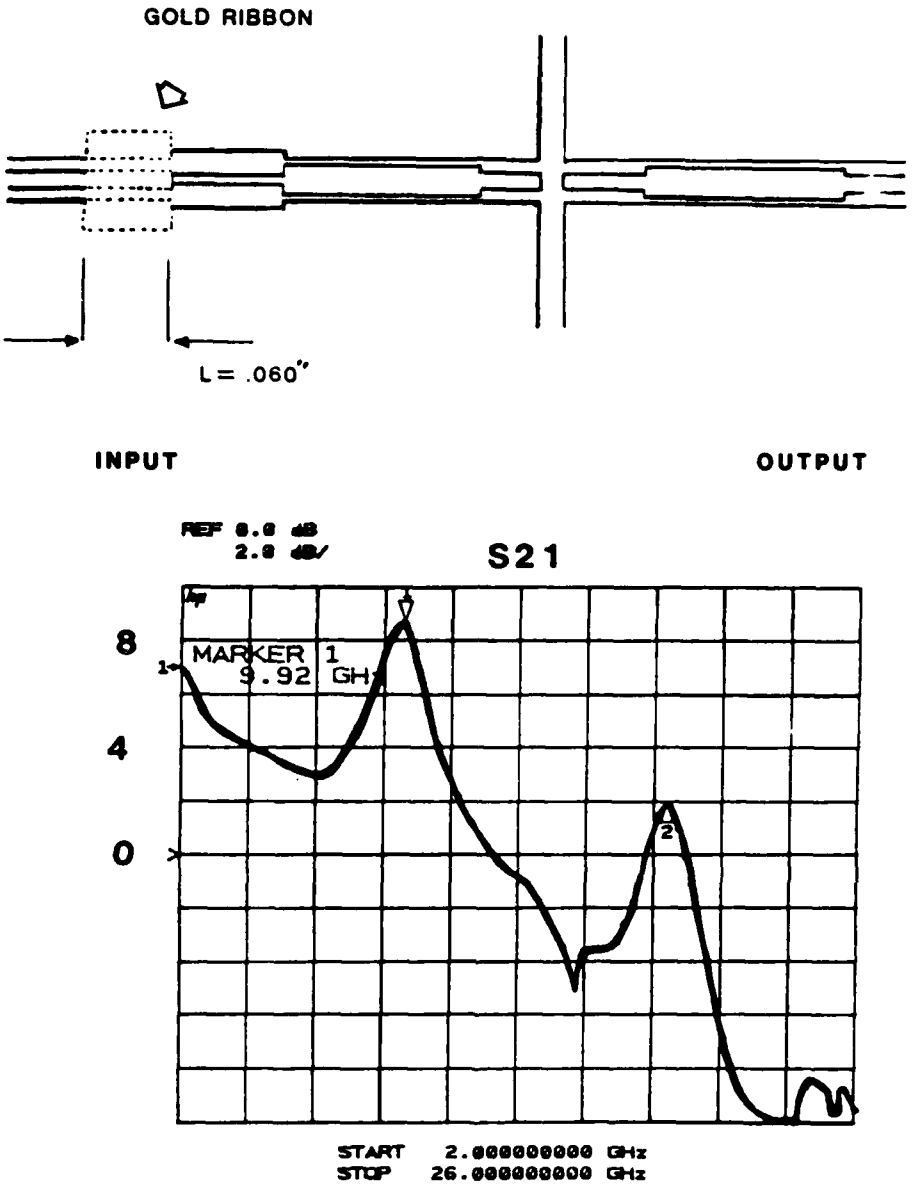


Figure 53. Location of Gold "Tweaking" Ribbons and the Effect of the Ribbons on the Performance of AMP1, as Measured on an HP-8510 Network Analyzer

The bottom of Figure 53 shows the performance of AMP2 with the ribbons added, as measured on an HP-8510 network analyzer. The gain peak is now at 9.92 GHz. Note the 2 dB gain peak at 20 GHz.

5.5 20 GHz Amplifier Design

5.5.1 SERIES DESIGN

Because the design of the 20 GHz amplifiers was based on incorrect s-parameters, and the final amplifiers did not behave as intended, the design of the amplifiers will only be discussed briefly.

The 1404 s-parameters used for the design indicated that the active device was stable for frequencies above 13.4 GHz. The gain and stability circles were not, therefore, required to design the amplifiers for maximum small-signal gain at 20 GHz. The use of the stability circles was only required below 13.4 GHz to ensure that the matching circuits were not capable of causing oscillations. At 20 GHz, the simultaneous conjugate match source and load reflection coefficients were:

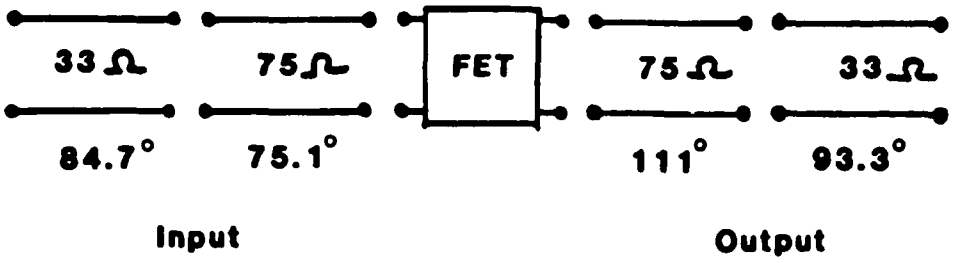
$$\Gamma_{MS} = 0.710 < 3.2° \tag{51}$$

$$\Gamma_{ML} = 0.677 < -44.1° . \tag{52}$$

The magnitudes of both the above reflection coefficients are both rather high. Figures 37 and 40 indicate that, for a range of CPW characteristic impedance between 30 Ω and 75 Ω, it was necessary to use a dual-section matching network to transform 50 Ω to the necessary Γ_{MS} and Γ_{ML}. The use of a Smith chart and the CIRCLES2 program indicated that a ZT1 section of 33 Ω and a ZT2 section of 75 Ω could be used to provide source and load reflection coefficients very close to those required for a simultaneous conjugate match. SUPERCOMPACT® was used to find the optimum electrical lengths of the dual-section matching circuits on the input and output of the amplifier, with the goal of realizing the MAG of 7.3 dB at 20 GHz. Figure 54a shows the basic dual-section 20 GHz amplifier design.

5.5.2 STUB DESIGN

An amplifier using parallel stubs was also designed. Although parallel stubs in CPW may not behave very well at 20 GHz, the author was curious to see how they would behave, and they were included in the photomask at no extra cost. Open stubs were used to avoid problems with biasing the active device. A simple Smith chart design was done using two 50-Ω open stubs on the input, and two 50-Ω open stubs on the output. SUPERCOMPACT® was used for optimization purposes.



DUAL-SECTION & DUAL-SECTION

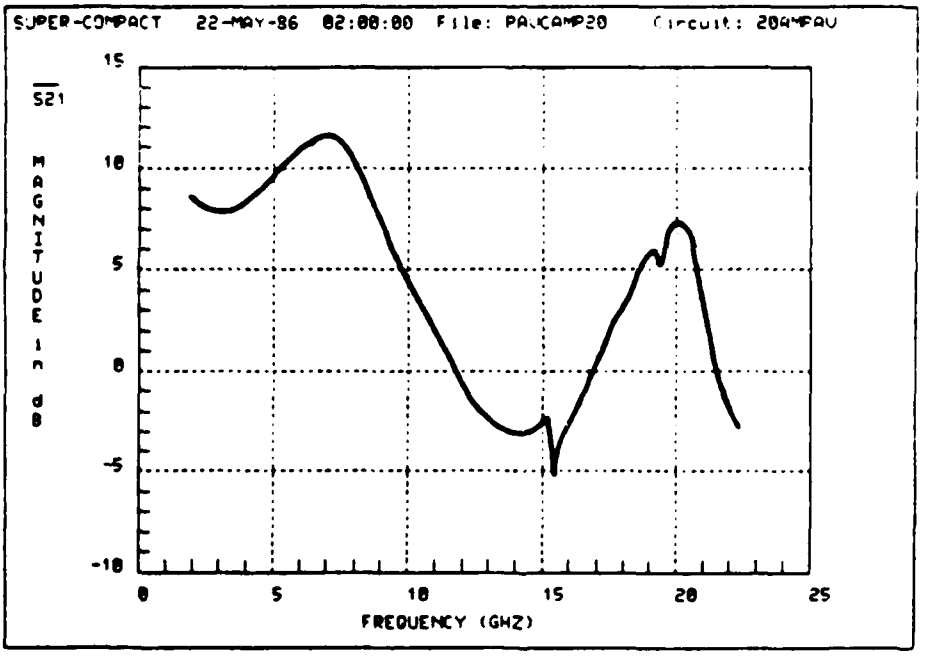


Figure 54. Design of 20 GHz CPW Amplifier Using Dual-section Matching Networks and SUPERCOMPACT® Prediction of Gain of Dual-section Design From 2 GHz to 22 GHz. Electrical lengths of transmission lines are for a frequency of 20 GHz

5.5.3 DISCONTINUITIES

It was expected that discontinuities in the distributed matching networks of the 20 GHz amplifiers would alter the behavior of the matching networks. In both the parallel and series element designs, approximate methods were used to

compensate for the discontinuities. Using SUPERCOMPACT®, the lengths of the open stubs were adjusted to account for the excess capacitance that would be present if the CPW stubs were terminated with 50-Ω microstrip opens. A microstrip open is probably only a crude approximation to a CPW open, but this approximation is the best that could be implemented quickly. No attempt was made to account for any parasitic reactances in the "T" junction where the stubs joint the center CPW conductor. In the construction of the stub amplifier, gold ribbons were used to bridge the stubs and maintain the ground plane continuity.

The discontinuities in the series transmission line network were assumed to behave as small parallel capacitances. The transmission line impedances used in the 20 GHz design were deliberately chosen to be equal to two of the transmission line impedances used in the 10 GHz design, in order to use the measured performance of the 10 GHz amplifier to determine approximate values of the parallel capacitors used to model the discontinuities in the 20 GHz design. The ANA VAR command was used on SUPERCOMPACT® to vary the values of the capacitors until the predicted performance of the 10 GHz amplifier agreed, as closely as possible, with the performance of the actual amplifier with and without the tuning ribbons in place. The appropriate capacitors were then included in the 20 GHz circuit on SUPERCOMPACT®, and the circuit optimized, using the electrical lengths of the transmission lines as the optimization variables, for the MAG at 20 GHz. Figure 54 shows the predicted performance of the 20 GHz amplifier dual-section design. The predicted performance of the stub design was very similar. Both amplifiers were designed using Keff values for the CPW line that were 5 percent higher than those calculated by SUPERCOMPACT®. A full-wave analysis of the S = 0.010 in., W = 0.007 in. 50-Ω line had shown this 5 percent difference to exist, and this value was used, as an approximation, for the other lines as well.

5.5.4 PERFORMANCE OF 20 GHz AMPLIFIERS

A total of three 20 GHz amplifiers were built—one of the stub-type design and two using the dual-section networks. None of the amplifiers provided any gain at 20 GHz. Figure 55 shows the performance of the stub amplifier and one of the dual-section amplifiers as measured on the HP 8510. Both the dual-section amplifiers had similar s-parameters. As mentioned in Section 4, a second de-embedding effort indicated that the 20 GHz amplifiers had been designed using s-parameters that were not representative of any of the other 1404 chips. Figure 56 is a plot of the simultaneous conjugate match source and load reflection coefficients calculated from both the s-parameters used to design the 20 GHz amplifiers and those obtained in the second de-embedding effort. The two circles labeled ZT1 and ZT2 show the matching circuit design. The curves labeled "DESIGN" were calculated

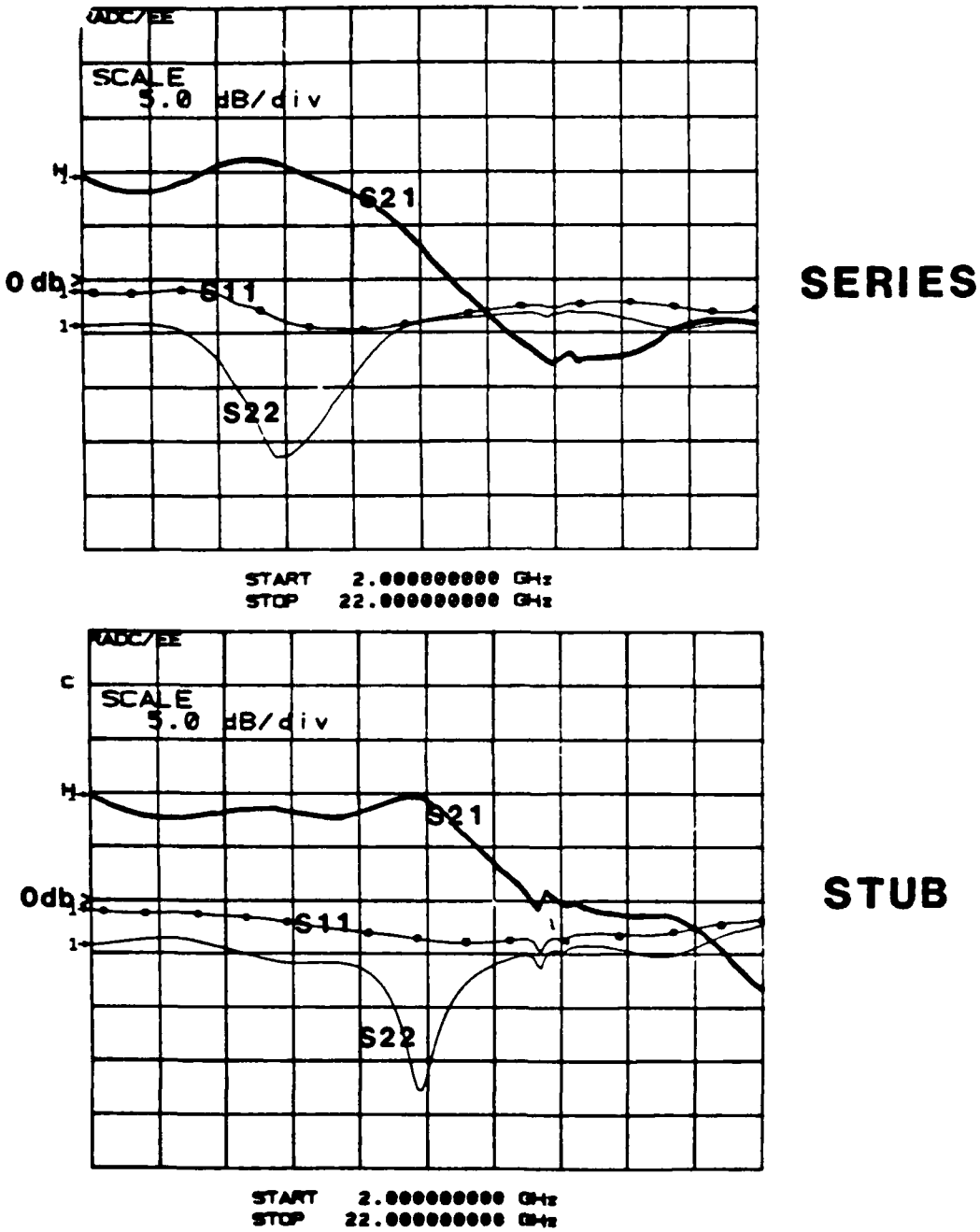


Figure 55. Performance of 20 GHz CPW Amplifiers as Measured on an HP-8510 Network Analyzer

from the s-parameters used to design the amplifiers, and the curves labeled "BUILD" were calculated from s-parameters obtained in the second de-embedding effort. The electrical lengths of the ZT1 and ZT2 sections

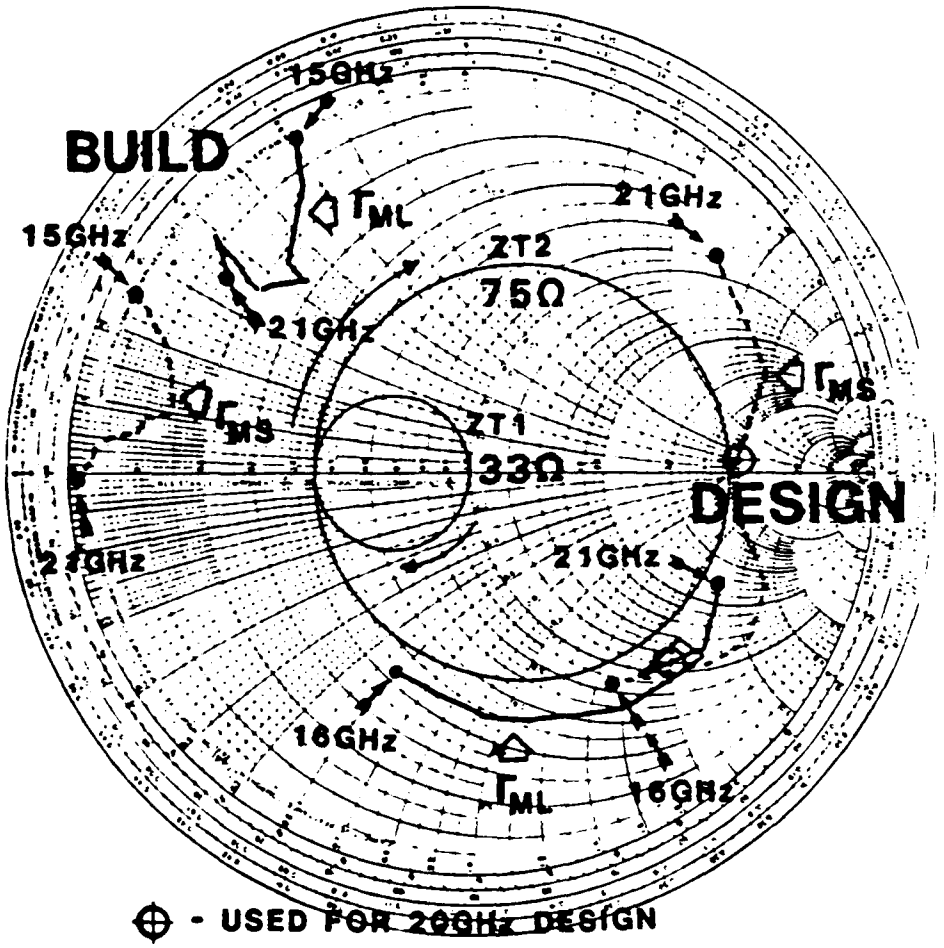


Figure 56. Simultaneous Conjugate Match Source and Load Reflection Coefficients Calculated From Both "DESIGN" and "BUILD" de-embedded s-parameters, and Reflection Coefficients Presented to FET by Dual-section Matching Circuit

were chosen to place the load and source reflection coefficients presented to the FET by the matching networks very close to the points marked 20 GHz on the simultaneous conjugate match load and source reflection coefficient curves. Notice, however, that the correct load and source reflection coefficients, necessary to provide the MAG at 20 GHz, are located virtually on the other side of the Smith chart from those presented to the device. This is the reason the 20 GHz amplifiers have approximately -5 dB gain at 20 GHz, rather than something closer to the MAG. Figures 57a and 57b contain a SUPERCOMPACT® prediction of the dual-section 20 GHz amplifier s-parameters when the "BUILD" s-parameters are used in the program instead of the "DESIGN" s-parameters, and also contains the de-embedded s-parameters of the dual-section amplifier. The predicted and

measured performance agree quite well, indicating that the s-parameters obtained in the second 1404 de-embedding effort are representative of those of the 1404 chips used to build the 20 GHz amplifiers.

FETX, one of the 1403 chips used to de-embed the s-parameters used in the 10 GHz design, was de-embedded using measurements taken on an 8510, yielding s-parameters up to 22 GHz. These s-parameters were used on SUPERCOMPACT® to predict the performance of the 10 GHz amplifier up to 22 GHz. The discontinuity capacitors were included in the model. Figure 58 is a plot of the $|S_{21}|$ predicted by SUPERCOMPACT® and the actual $|S_{21}|$ of the lower gain 10 GHz amplifier as measured on the HP 8510. The two curves agree rather well, but the gain peaks near 20 GHz do not coincide exactly. De-embedding the S_{21} of the 10 GHz amplifier may have helped eliminate the frequency difference between the measured and predicted gain peaks, but the author could not have easily done this at the time.

The author feels that the techniques used in this project are adequate to predict, with a reasonable amount of success, the performance of CPW circuits up to a frequency of at least 20 GHz.

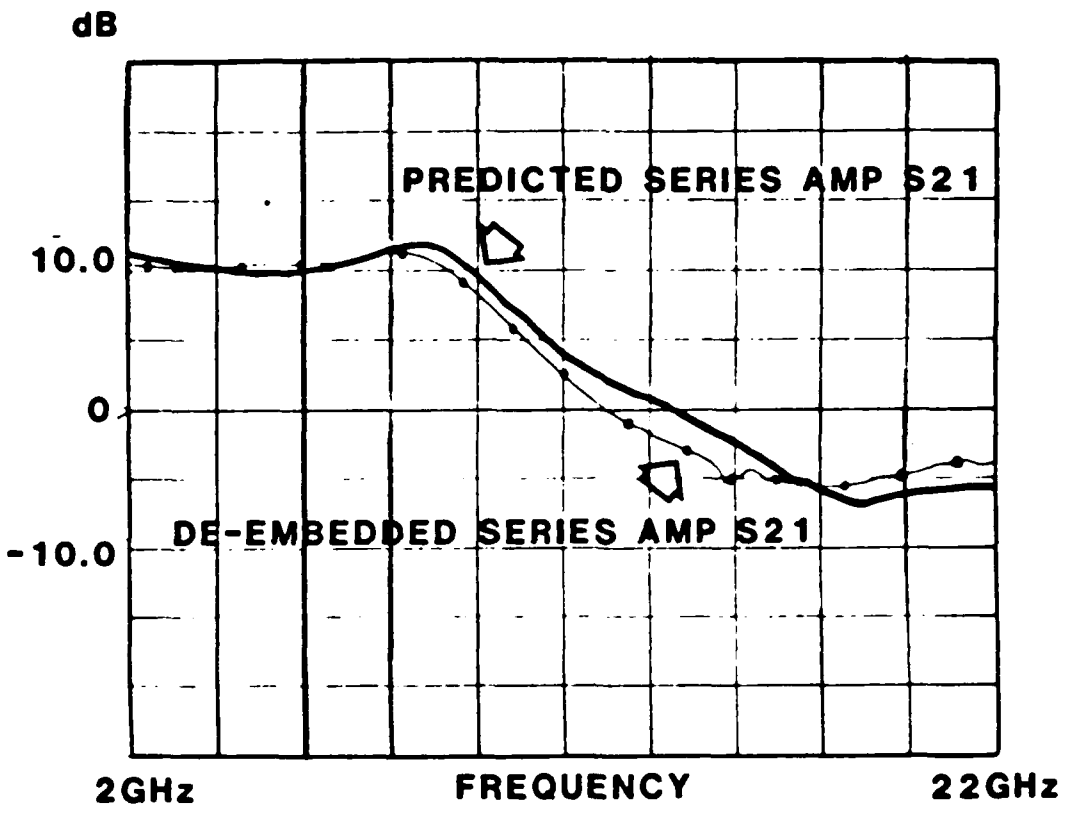


Figure 57a. SUPERCOMPACT® Prediction of Gain of Dual-section 20 GHz CPW Amplifier With "BUILD" s-parameters in Program, and De-embedded Gain of Actual Dual-section 20 GHz CPW Amplifier. Data taken on an HP-8510 network analyzer

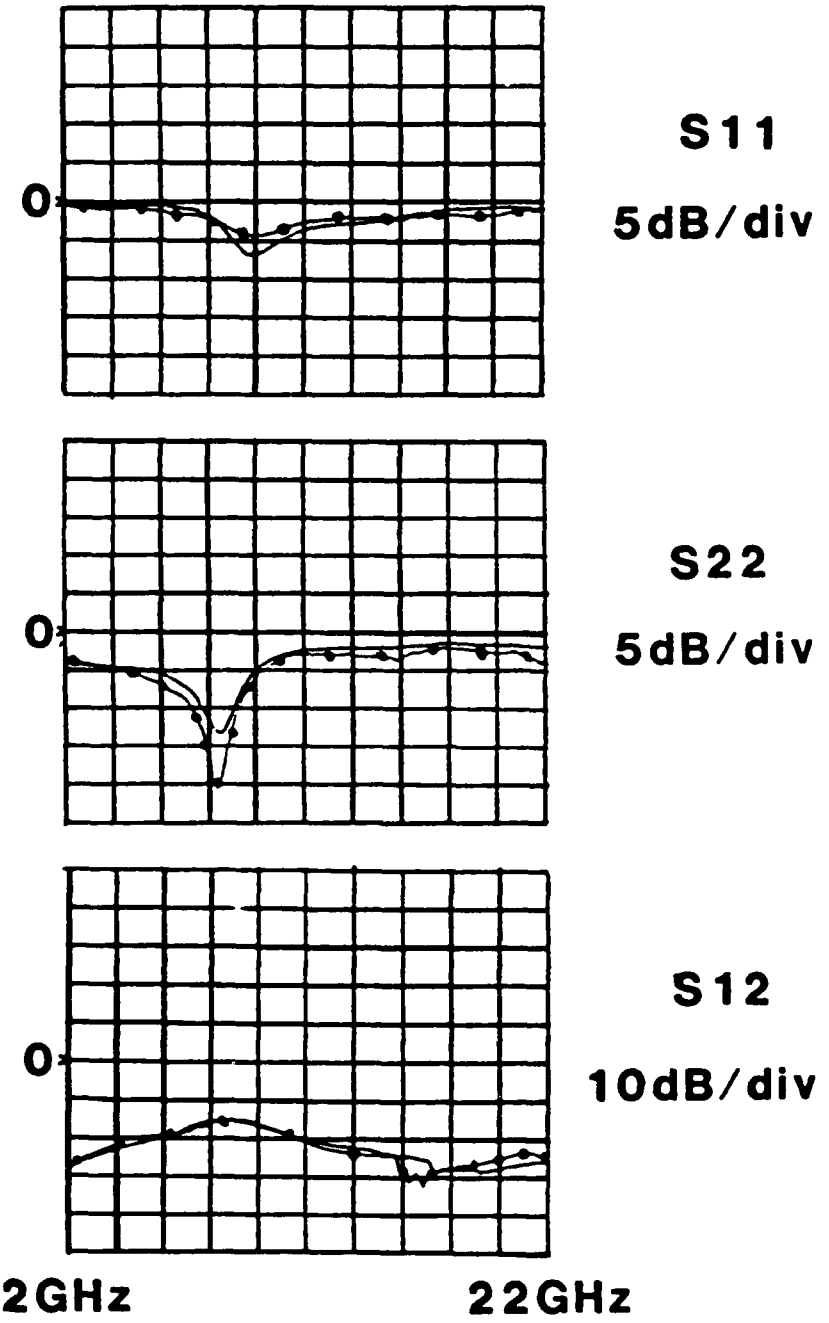


Figure 57b. SUPERCOMPACT® Prediction of S_{11}, S_{22}, and S_{12} of Dual-section 20 GHz CPW Amplifier With "BUILD" s-parameters in the Program and De-embedded S_{11}, S_{22}, and S_{12} of Actual Dual-section 20 GHz CPW Amplifier

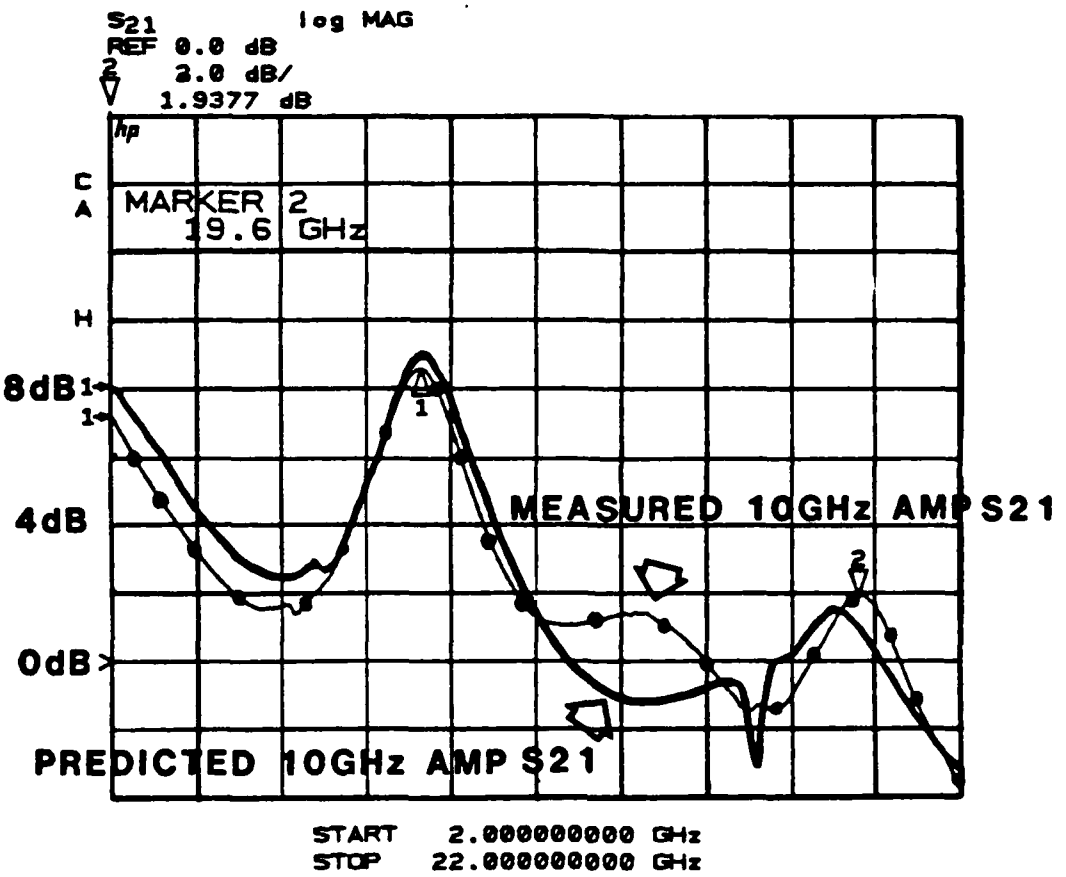


Figure 58. SUPERCOMPACT® Prediction of Gain of the 10 GHz CPW Amplifier Using the De-embedded s-parameters of FETX in the Program, and the Actual Gain of the 10 GHz CPW Amplifier as Measured on an HP 8510 Network Analyzer. Amplifier gain is not de-embedded

6. CONCLUSIONS AND RECOMMENDATIONS

6.1 20 GHz Amplifier

If the s-parameters obtained in the second 20 GHz de-embedding effort had been used to design the 20 GHz amplifier, the author believes that amplifiers with gain peaks fairly close to 20 GHz could have been fabricated. The successful prediction by SUPERCOMPACT® of the actual performance of the 20 GHz amplifiers and of the behavior of the 10 GHz amplifier at 20 GHz indicates that all the techniques used in this report, including the de-embedding method, the type of test fixtures developed, and the series transmission line matching networks, can be used to design and build circuits at 20 GHz. However, the discontinuities in the CPW matching circuits would have probably caused a slight frequency shift in the response of any 20 GHz final circuits, even after modelling the discontinuities with the parallel capacitors. It would be very helpful if discontinuities in

CPW were to be successfully characterized by theorists, and routines for including discontinuities incorporated into a CAD program such as SUPERCOMPACT®.

6.2 Data Acquisition

The use of automated data acquisition techniques can greatly speed the overall research and design process by increasing the number of design and test iterations possible in a given period of time. For instance, in de-embedding the s-parameters of the FET chips used in this project, measurements often had to be taken several times before data that the author felt confident about could be obtained. A slightly loose connector or a cracked epoxy connection prevented at times the successful de-embedding of the s-parameters of a chip, but this was usually only evident after at least one failed de-embedding attempt, and a subsequent thorough search for a cause of the bad s-parameters. Regardless of how skilled a particular researcher is, design work at frequencies such as 20 GHz seems to require a few design and test iterations before particular device or design can be made to work correctly, or shown to be completely unworkable.

The author found two programs written by Gary Scalzi at RADC to be extremely useful and to contribute to a more efficient research effort. Menus from each of the programs, listing the options available to a user and indicating the capabilities of each of the programs, are reproduced in Figure 59. The important items on the menus are more or less self-explanatory. The real time de-embedding and embedding option on the second menu promises to be very helpful in the future.

```
INTERFACE : HP8510 NETWORK ANALYZER <----> VAX 11/730

  1  UPLOAD CORRECTED DATA FILES FROM 8510 TAPE TO VAX [default]
  2  UPLOAD UNCORRECTED RAW DATA FILES, COMPUTE & DOWNLOAD ERROR TERMS
  3  UPLOAD ERROR TERMS FROM 8510 MEMORY
  4  DOWNLOAD DATA FILE FROM DISK TO 8510 TAPE FILES
  5  DOWNLOAD ERROR TERMS FROM DISK TO 8510 MEMORY
  6  CONVERT 1-PORT BOND WIRE FILE TO 2-PORT BOND WIRE FILE
  7  PERFORM OFF-LINE DEEMBEDDING
 88  HELP
 99  EXIT PROGRAM

CHOICE >


MENU

  1  DE-EMBED 2 NETWORKS FROM DUT MEASUREMENT [default]
  2  EMBED 2 NETWORKS INTO A DUT MEASUREMENT
  3  CONVERT ERROR TERMS FOR REAL-TIME DE-EMBEDDING
 99  EXIT PROGRAM

CHOICE >
```

Figure 59. Menus From Computer Programs Used for Data Acquisition

6.3 De-embedding

There are a few ways in which the de-embedding method can be improved. Measurements of lengths inside the test fixtures and of the overall lengths of the fixtures are important in the de-embedding process. De-embedding removes the electrical effects of the K-connector-to-CPW transitions and a certain lengths of CPW line from a measurement of a FET chip in a test fixture, but, in this project, the resulting s-parameters still included small lengths of transmission line attached to the input and output of the chip. Optimally, the length of the test fixture containing the FET chip should be greater than the length of the short fixture (THRUS) by the length of the FET chip and the input and output bond wires. The reference plane of the de-embedded s-parameters is then automatically established right at the point where the bond wires contact the CPW. Because the test fixtures containing the FET chips were not of the optimum length described above, the program FTDMBED was modified to allow for a reference plane shift of the error terms before using them to de-embed the chip. The problem, however, was in determining the exact lengths of transmission line, and thus amount of reference plane shift, to include in FTDMBED. The author assumed that the groove containing the FET was in the middle of the substrate, distributed any excess length between the fixture containing the chip and THRUS evenly on each side of the chip, and used these transmission line lengths in FTDMBED. In the future, it is suggested that the test fixture containing the chip be made the optimum length, or more precise methods be used to measure lengths inside the fixtures. At 20 GHz, a 0.005 in. uncertainty in the location of a reference plane can make a 16° difference in the phase of S_{11} or S_{22}, assuming a 50-Ω CPW line of the dimensions used in this project on a substrate of an effective dielectric constant of 13. At a frequency of 35 GHz, the difference is about 27°. An amplifier design based on de-embedded s-parameters that contain a phase error can cause the response of the actual amplifier to be shifted in frequency from that intended in the design.

The FET-in-Groove mounting technique was difficult to use and other techniques for mounting the FET chip should probably be investigated. It is possible to ultrasonically drill a hole the size and shape of a FET chip into ceramic material. The method was described to the author by engineers at MPC Inc. of Lowell, Massachusetts. The hole can be precisely located, and if its size was chosen to be close to that of the FET chip, very short bond wires would suffice to electrically connect the chip to a CPW line. Another possibility for mounting the chip is to simply place it on top of the substrate and use small gold-plated "pedestals" to raise the ground plane and center conductors to the level of the chip, and to use bond wires to connect the chip to the "pedestals." The "pedestals" could be attached to the CPW lines with silver epoxy. Of course, in a fully monolithic

design, as is currently underway at RADC, these chip mounting considerations do not apply.

6.4 Future Work

The next logical step is to build fully monolithic amplifiers, rather than continue with any hybrid-type construction techniques. The author is currently involved in the design of GaAs, fully monolithic amplifiers using CPW transmission lines. Both power and low-noise amplifiers are being designed, and most of the work, including the actual fabrication of active devices, is to be done in-house at RADC. A comparison between the performance of the hybrid amplifiers described in this report and the fully monolithic amplifiers to be constructed is planned for the future.

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